ERRATA FOR EDITION 3

PLEASE SEND ANY OTHER ERRATA TO res@ece.ubc.ca.

1. p. 6, in Table 1.1, place the term **thin-oxide gate leakage** under the term hot-carrier effects in the column marked DSM Devices.

2. p. 34, in problem P1.11, "… will it take for **processors** speeds to reach **30**GHz?" should be replaced with "…will it take for **processor** speeds to reach **10**GHz?"

3. p. 47, 2nd last line before Example 2.1, "*n*-type source **for**" should be replaced with "*n*-type source **or**"

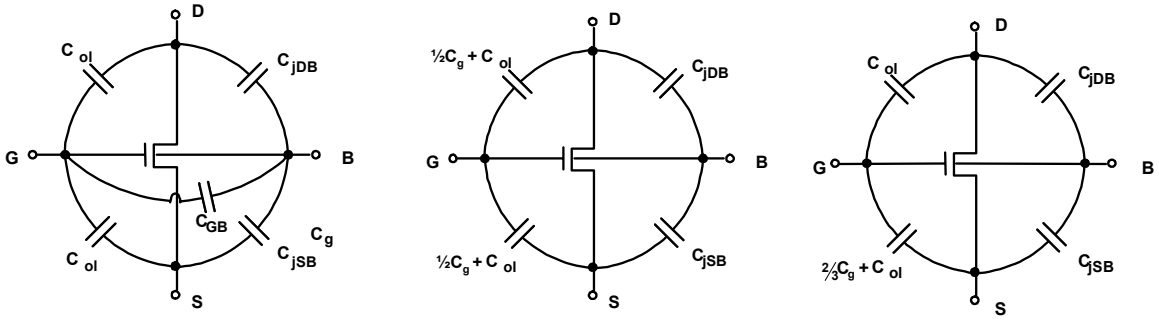
4. p. 70, top line should read: $\Delta V_{GS} = V_{GS1} - V_{GS2}$

5. p. 78, in Example 2.12, replace "*" with "x" in the equation underneath the square root sign just above the word "Problem:". This is just a type-setting error.

6. p. 81 at the bottom should read " If $V_{GS} \geq V_T$" and the top of p. 82 should read "If $V_{GS} < V_T$"

7. p. 82, change Cutoff region term to $1/(1/C_g + 1/C_{jc})$ in 3rd line from bottom of page.

8. p. 83, the last figure for the capacitances should have 2/3 Cg + Col for the gate-to-source capacitance, and Col for the gate-to-drain capacitance. New figure is as follows:

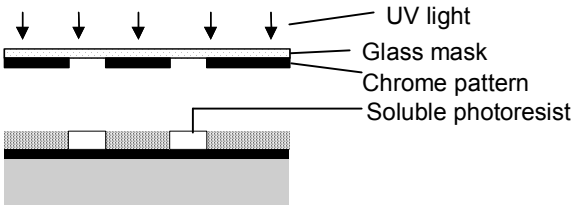


9. p. 85, in P2.8, replace "*" with "x" in the expression for υ_{sat}. This is just a type-setting error.

10. p. 85, in P2.8, at the end of the parameter list, add ", $\lambda=0.7V^{-1}$."

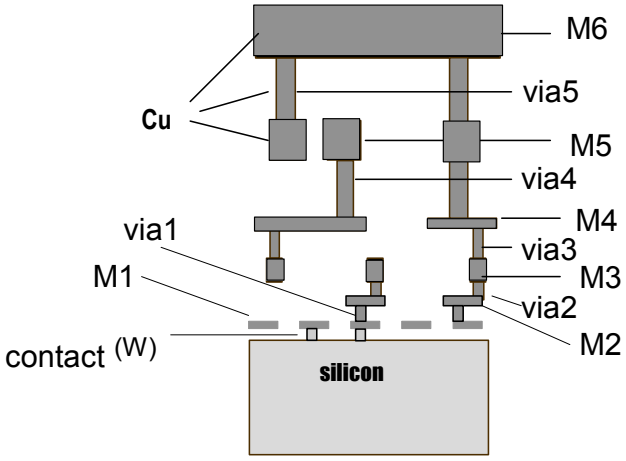
11. p. 92, at the end of the page, replace "Step 1: Apply material to **water**" with "Step 1: Apply material to **wafer**"

12. p. 93 – the soluble photoresist extends further than appropriate. The correct figure is



Step 3: Pattern photoresist with UV light through glass mask

13. p. 99, Figure 3.3 should be all copper with stacked vias as follows :



14. p 123 , d=4 should be replaced with pd=4 in the SPICE line for mp

15. p 126, s=8 should be replaced with as=8 in the SPICE line for mp

16. p. 146, Figure 4.2, remove label "V_{DD}" that occurs just above V_{in} and under the text "Low gain". Also, the dotted line for V_{OL} should line up with solid curve. Currently it shows up just above the solid line where "Low gain" is referenced.

17. p. 157, middle of the page. Replace "The value of $\mathbf{V_{OUL}}$ can be determined by by substituting $V_{in} = V_{IL}$ into Equation **(4.6b)** and solving for V_{out}, if needed." with the statement "The value of $\mathbf{V_{OUH}}$ can be determined by by substituting $V_{in} = V_{IL}$ into Equation **(4.8a)** and solving for V_{out}, if needed."

18. p. 162, Figure 4.10(c) is missing a V_{IL} label in the graph

19. p. 173, near the bottom of the page, replace $V_{out}=V_{OUL}$ with $V_{out}=V_{OUH}$.

20. p. 174, near the bottom of the page, replace $V_{out}=V_{OUH}$ with $V_{out}=V_{OUL}$.

21. p. 179, the expression for V_{OL} in the middle of the page should have "=" replaced with "≅".

22. p. 187-188, Figures P4.1 and P4.2 should be reversed.

23. p. 263, for the SPICE file, m3 should have "**pd=80 ps=80"** replaced with "**pd=160 ps=160"** at the end of the line

24. p. 263, for the SPICE file, m5 should have "**pd=320 ps=320"** replaced with "**pd=640 ps=640"** at the end of the line

25. p. 273, 2nd last line of page in Example 6.6, replace **5.4fF** with **10.8fF**

26. p. 276, third line of 1st paragraph, replace "…such ramp inputs…" with "…such **as** ramp inputs…"

27. p. 280, Figure 6.22 caption should replace "**NAND gates"** with "**inverters"**

28. p. 286, the Fanout_delay equation in the solution has a correction in the 2nd step as follows (i.e., the term $R_{eqn}C_gL_n$ should not be under the square-root sign):

$$Fanout\_delay = \sqrt[3]{\tau_{nand}\left(\frac{C_{j+1}}{C_{IN}}\right)\times\tau_{inv}\left(\frac{C_{j+2}}{C_{j+1}}\right)\times\tau_{nor}\left(\frac{C_{load}}{C_{j+2}}\right)}$$

$$= \sqrt[3]{\tau_{nand}\times\tau_{inv}\times\tau_{nor}\left(\frac{C_{load}}{C_{IN}}\right)} = \sqrt[3]{3\times4\times5\left(\frac{200}{2}\right)}\times R_{eqn}C_gL_n$$

$$= 18.2R_{eqn}C_gL_n$$

29. p. 286, the first "=" sign in the equation starting with τ_{inv} should be removed.

30. p. 291, replace Table 6.2 entries as follows:

Table 6.2:

Table of parasitic terms for simple gates

Type of Gate	**1 input**	**2 inputs**	**3 inputs**	**4 inputs**
Inverter	0.5	-	-	-
NAND	-	1	2	3
NOR	-	1.5	3	4.5

31. p. 296, as a side effect of the above change, some numbers in Example 6.14 change. In the first equation for D, change the parasitic term for the NAND4 to **3** (instead of **2**):

$$D = 4(Path\ Effort)^{1/4} + \sum P = 4((2)(4/3)(10))^{1/4} + 3 + 1/2 + 1 + 1/2 = 14$$

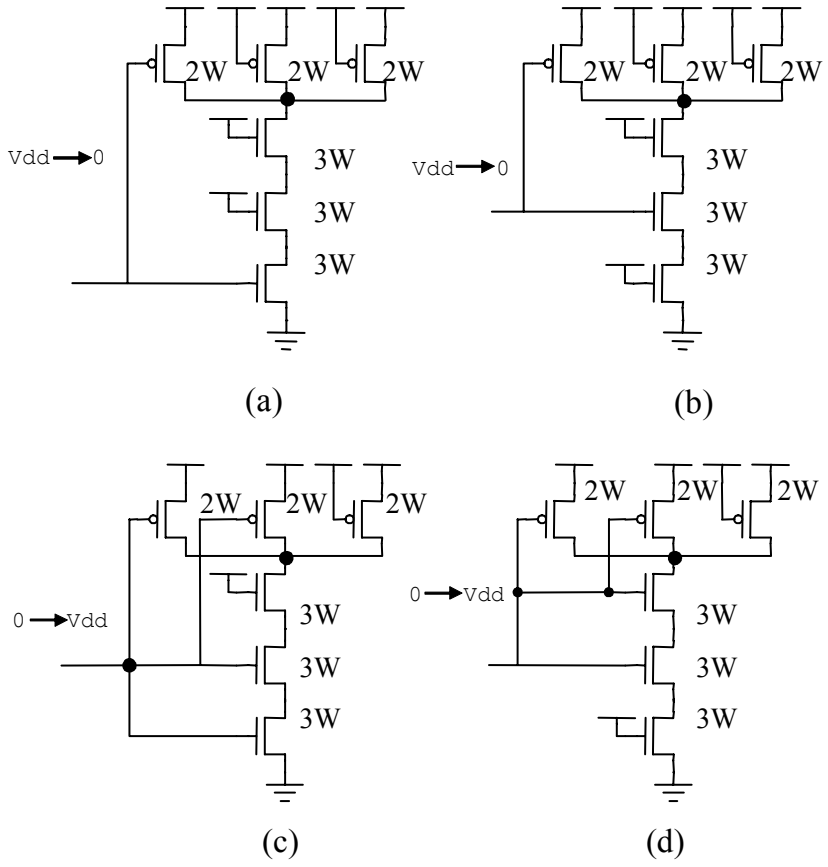
32. p. 297, as a side effect of the change of Table 6.2, the first statement should read:

Option 2 is better than option 1.

33. p. 302, Path Effort equation near the bottom of the page should have one "+" replace with a "x" as follows:

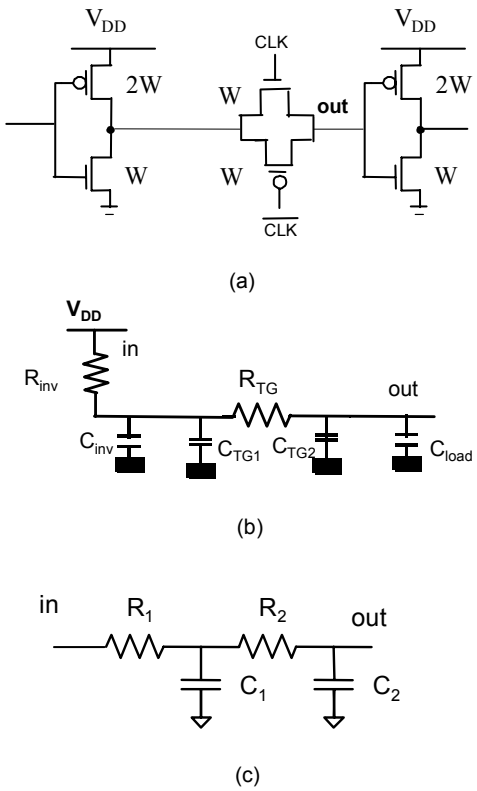
$$D = \sum (LE \times BE + P)$$

34. p. 304, for clarity, the figures in P6.4 should be shown as follows:

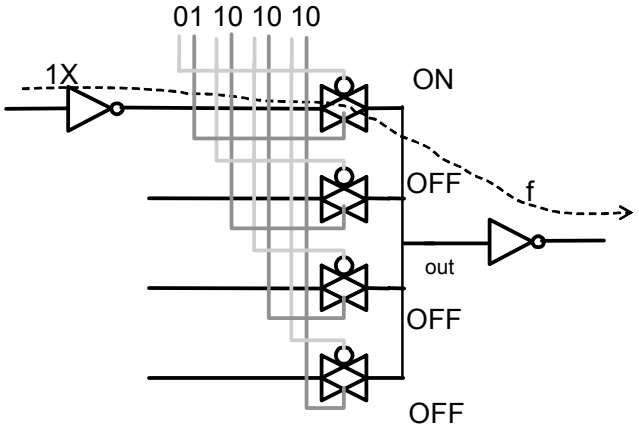


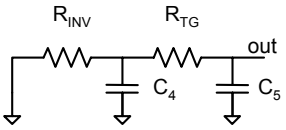
35. p. 307, replace "**LE_R**" with "**rising LE_R**", and also replace "**LE_F**" with "**falling LE_F**". Furthermore, Figure P6.10 should have the label *F* removed from the output of the schematic. This is confusing for the reader due to the use of LE_F.

36. p. 329, Figure 7.18(a) should have a label “Out” as shown below:



37. p. 329, Figure 7.18(a) should have label “**out**” just before the 2nd inverter as shown below (it should *not be after* 2nd inverter as given in the text):





$t_2 = R_{INV}C_4 + R_{TG}C_5$

$C_4 = 3C_{eff}W + 2C_{eff}W + C_gW$

$C_5 = 2C_{eff}W \times 4 + C_gW + 3fC_gW$

$t2 = R(21C_{eff} + 3C_g + 6fC_g)W$

$R_{inv}=R$ $R_{TG}=R$

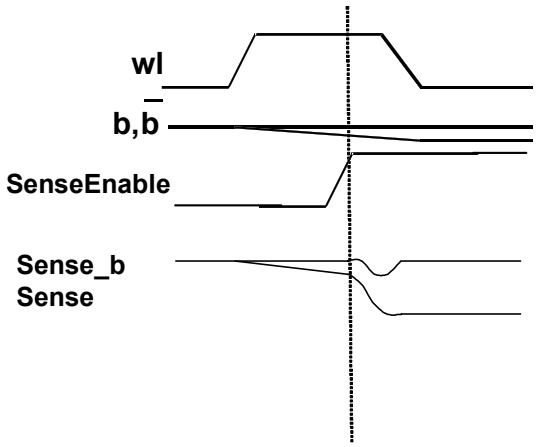
38. p. 352, Problem P7.3(b) replace "**capcitance**" with "**capacitance**" in third line. This is a spelling error.

39. p. 357, Problem P7.15, in 2nd line, replace "**… an addition transistor**" with "**… an additional transistor**"

40. p. 383, In Figure 8.18, the labels of q and $\overline{q}$ should be reversed on the waveform diagram.

41. p. 387, the last sentence should be deleted and replaced with "**Eventually, the pull-down transistors on one side act to bring down the output to Gnd while, on the other side**,". Note that this sentence will run on to the top of p. 388 which should remain unchanged as "**the pull-up transistor acts to raise the voltage to V_{DD}**". Delete the word **regenerative** in the next sentence.

42. p. 388, the last waveform in Figure 8.22 should be slightly separated from the other one as shown below:



Everything else in the entire figure should REMAIN exactly as before. Just change the lower waveform so that it gradually going down as indicated above.

43. p. 395, in DESIGN PROBLEM 1, 3rd paragraph, replace **5 fF** with **10 fF**. Delete the line that says "You can assume that the clock period is 24 FO4 delays".

44. p. 438, Problem P9.6, last line should read "**…must span at least two PLBs"**.

45. p. 439, P9.11, switch the positions of EPROM and E^2PROM. The question should read as follows:

P9.11. Explain why the select transistor is needed in an E^2PROM cell? How does the EPROM cell avoid the need for this extra transistor?

46. p. 452, Example 10.3, in last line replace **(1pf)** with **(1pF)** for the 2nd occurrence in the equation.

47. p. 494, the last equation should be $C_{decap} = C_{ox}WL + \mathbf{2}C_{ol}W$.

48. p. 525, Problem P11.3, all capacitances should be 5pF.

49. p. 525, Problem P11.4, add the following question at the end: "**Also, what is the minimum clock cycle?"**

50. p. 534, Indent the SPICE line starting with the label "Mn". It is out too far.

51. p. 560, last paragraph, 2nd and 3rd lines are missing "=" after I_{C2} and "-" after the 5. For clarity, the two lines are completely reproduced in their correct form below:

Consequently, for $V_{BE3} = V_{BE(on)} = 0.7$ V, $I_{C2} = I_{E2} = 0.7$ V/1 kΩ = 0.7 mA. The voltage at the collector of Q_2 is $V_{C2} = V_{CC} - I_{C2}R_3 = 5 - (0.7)(1.6) = 3.9$ V.

52. p. 563-580, miscellaneous index updates

53. BACK COVER, in second paragraph, on second line, change **.018μm** to **0.18μm.**

54. INSIDE FRONT COVER, last line should read: Wire Inductance L_{eff} **0.4-0.5** pH/μm