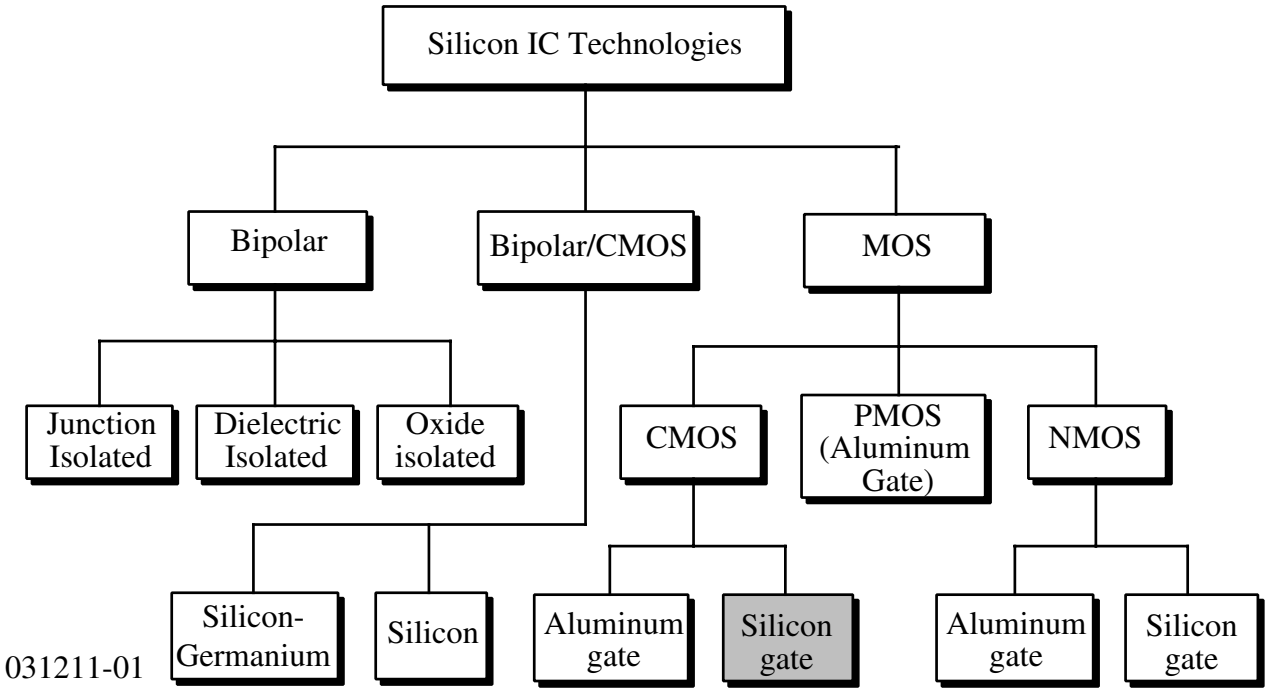
CMOS TECHNOLOGY

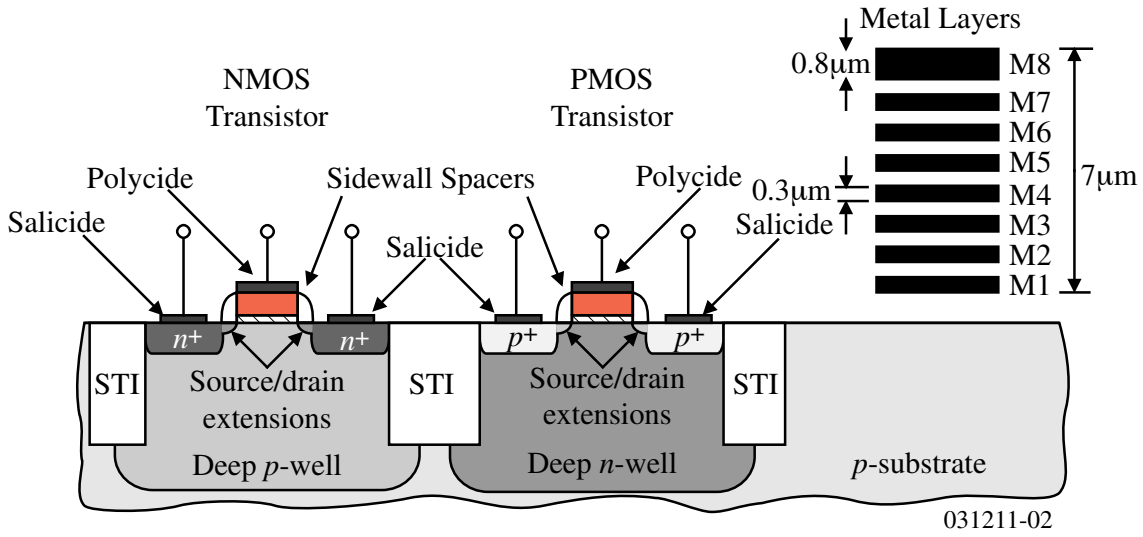
INTRODUCTION

Classification of Silicon Technology



Components of a Modern CMOS Technology

Illustration of a modern CMOS process:



In addition to NMOS and PMOS transistors, the technology provides:

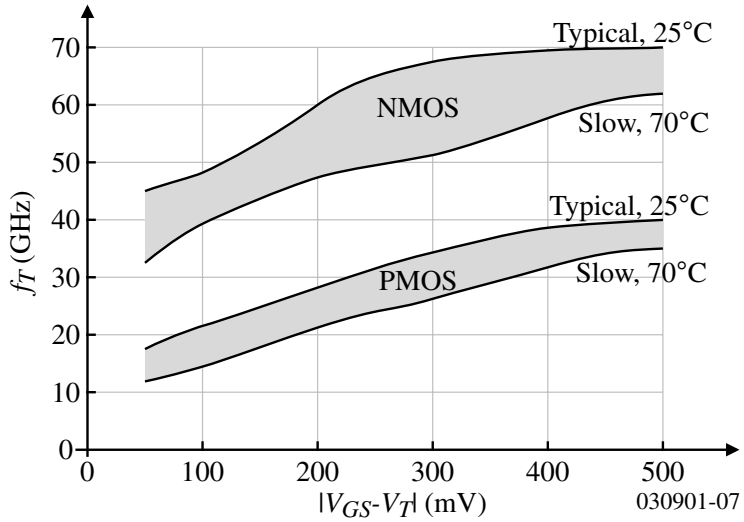
1.) A deep *n*-well that can be utilized to reduce substrate noise coupling.

2.) A MOS varactor that can serve in VCOs

3.) At least 6 levels of metal that can form many useful structures such as inductors, capacitors, and transmission lines.

CMOS Components – Transistors

f_T as a function of gate-source overdrive, V_{GS}-V_T (0.13μm):



The upper frequency limit is probably around 40 GHz for NMOS with an f_T in the vicinity of 60GHz with an overdrive of 0.5V and at the slow-high temperature corner.

FUNDAMENTAL PROCESSING STEPS

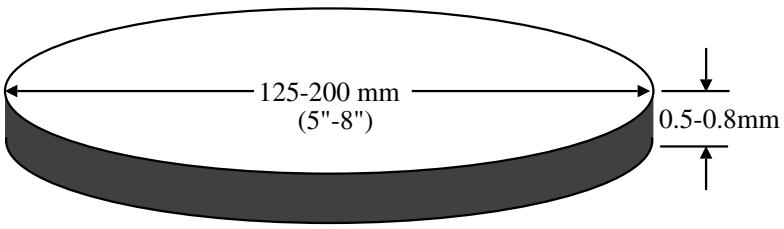
Basic steps

- Oxide growth
- Thermal diffusion
- Ion implantation
- Deposition
- Etching
- Epitaxy

Photolithography

Photolithography is the means by which the above steps are applied to selected areas of the silicon wafer.

Silicon wafer



n-type: 3-5 Ω-cm
p-type: 14-16 Ω-cm

Fig. 2.1-1r

Oxidation

Description:

Oxidation is the process by which a layer of silicon dioxide is grown on the surface of a silicon wafer.

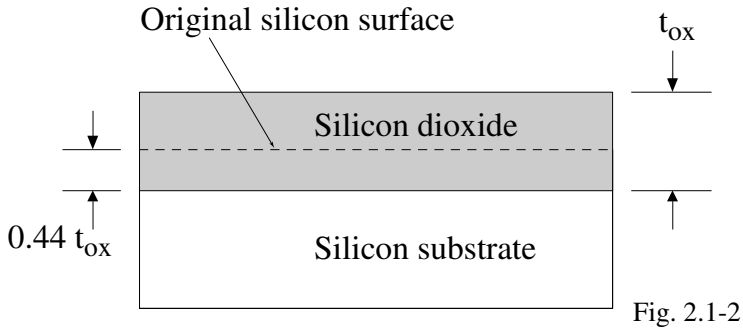


Fig. 2.1-2

Uses:

- Protect the underlying material from contamination
- Provide isolation between two layers.

Very thin oxides (100Å to 1000Å) are grown using dry oxidation techniques. Thicker oxides (>1000Å) are grown using wet oxidation techniques.

Diffusion

Diffusion is the movement of impurity atoms at the surface of the silicon into the bulk of the silicon.

Always in the direction from higher concentration to lower concentration.

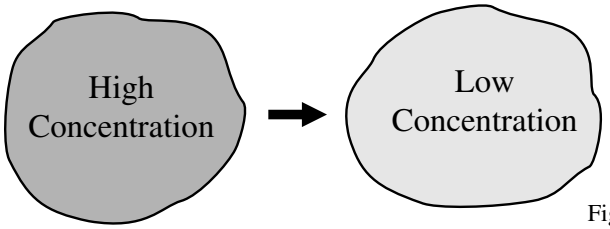
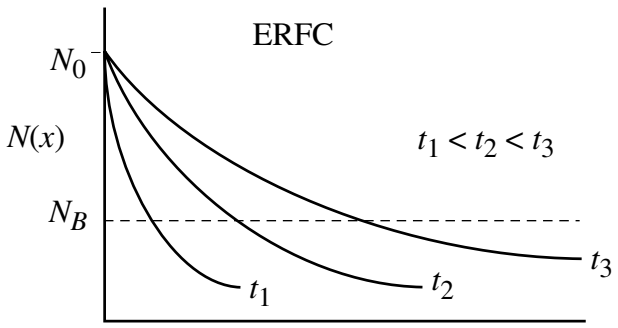
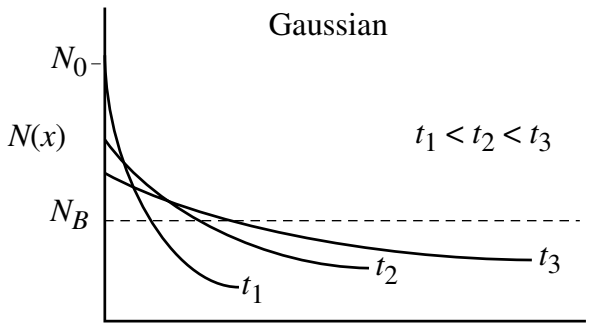


Fig. 150-04

Diffusion is typically done at high temperatures: 800 to 1400°C



Infinite source of impurities at the surface.



Finite source of impurities at the surface.

Fig. 150-05

Ion Implantation

Ion implantation is the process by which impurity ions are accelerated to a high velocity and physically lodged into the target material.

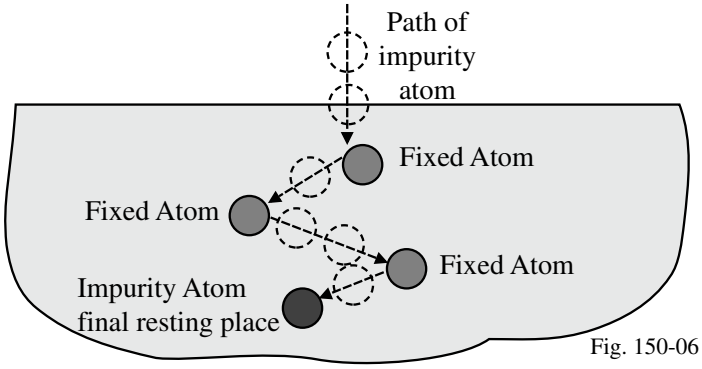


Fig. 150-06

- Annealing is required to activate the impurity atoms and repair the physical damage to the crystal lattice. This step is done at 500 to 800°C.
- Ion implantation is a lower temperature process compared to diffusion.
- Can implant through surface layers, thus it is useful for field-threshold adjustment.
- Can achieve unique doping profile such as buried concentration peak.

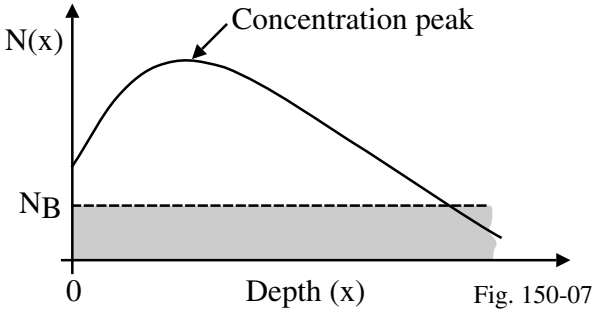


Fig. 150-07

Deposition

Deposition is the means by which various materials are deposited on the silicon wafer.

Examples:

- Silicon nitride (Si_3N_4)
- Silicon dioxide (SiO_2)
- Aluminum
- Copper
- Polysilicon

There are various ways to deposit a material on a substrate:

- Chemical-vapor deposition (CVD)
- Low-pressure chemical-vapor deposition (LPCVD)
- Plasma-assisted chemical-vapor deposition (PECVD)
- Sputter deposition

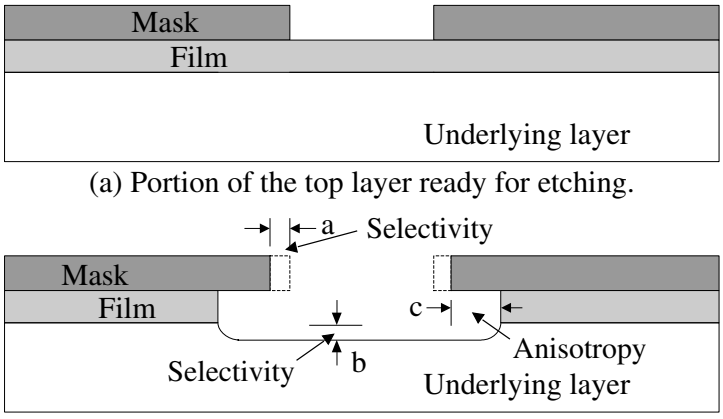
Material that is being deposited using these techniques covers the entire wafer.

Etching

Etching is the process of selectively removing a layer of material.

When etching is performed, the etchant may remove portions or all of:

- The desired material
- The underlying layer
- The masking layer



(a) Portion of the top layer ready for etching.

(b) Horizontal etching and etching of underlying layer.

Fig. 150-08

Important considerations:

- *Anisotropy* of the etch is defined as,

  A = 1-(lateral etch rate/vertical etch rate)

- *Selectivity* of the etch (film to mask and film to substrate) is defined as,

$$S_{film\text{-}mask} = \frac{\text{film etch rate}}{\text{mask etch rate}}$$

A = 1 and $S_{film\text{-}mask} = \infty$ are desired.

There are basically two types of etches:

- Wet etch which uses chemicals
- Dry etch which uses chemically active ionized gases.

Epitaxy

Epitaxial growth consists of the formation of a layer of single-crystal silicon on the surface of the silicon material so that the crystal structure of the silicon is continuous across the interfaces.

- It is done externally to the material as opposed to diffusion which is internal
- The epitaxial layer (epi) can be doped differently, even oppositely, of the material on which it grown
- It accomplished at high temperatures using a chemical reaction at the surface
- The epi layer can be any thickness, typically 1-20 microns

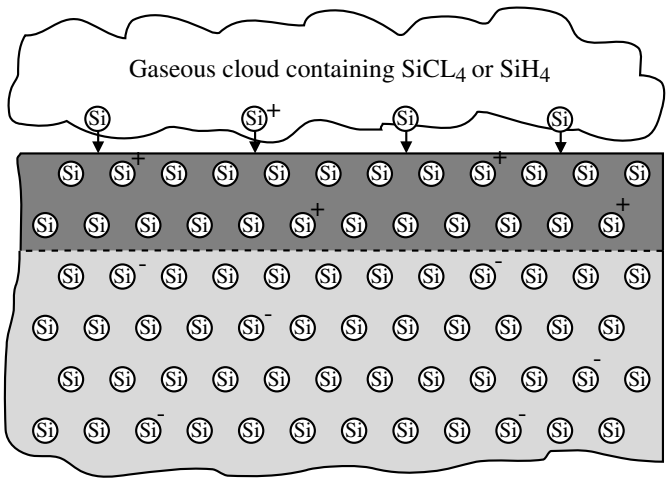


Fig. 150-09

Photolithography

Components

- Photoresist material
- Mask
- Material to be patterned (e.g., oxide)

Positive photoresist

Areas exposed to UV light are soluble in the developer

Negative photoresist

Areas not exposed to UV light are soluble in the developer

Steps

1. Apply photoresist
2. Soft bake (drives off solvents in the photoresist)
3. Expose the photoresist to UV light through a mask
4. Develop (remove unwanted photoresist using solvents)
5. Hard bake (≈ 100°C)
6. Remove photoresist (solvents)

Illustration of Photolithography - Exposure

The process of exposing selective areas to light through a photo-mask is called *printing*.

Types of printing include:

- Contact printing
- Proximity printing
- Projection printing

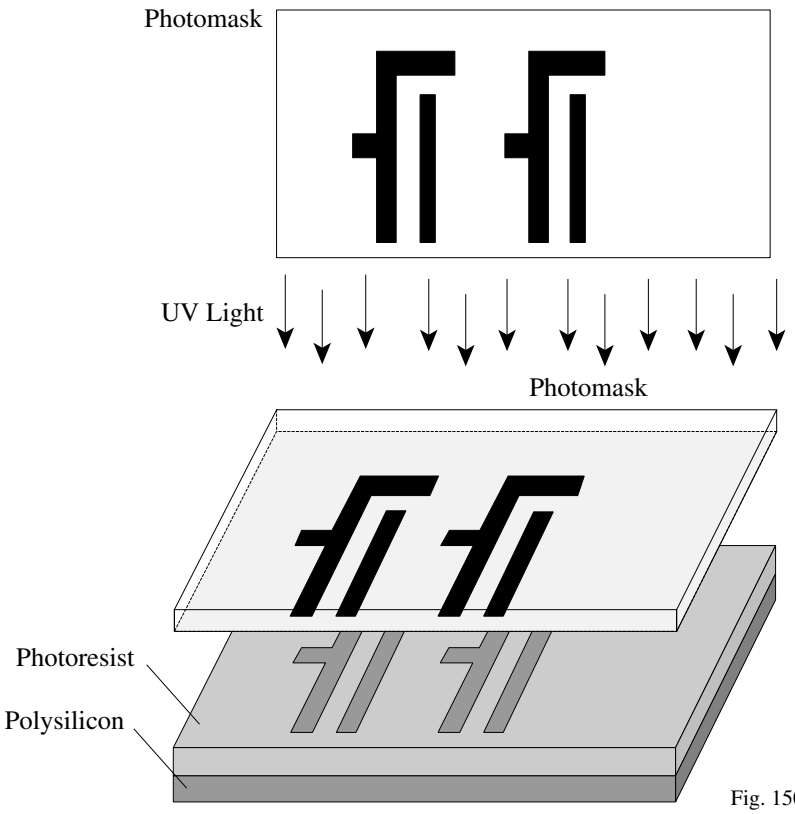


Fig. 150-10

Illustration of Photolithography - Positive Photoresist

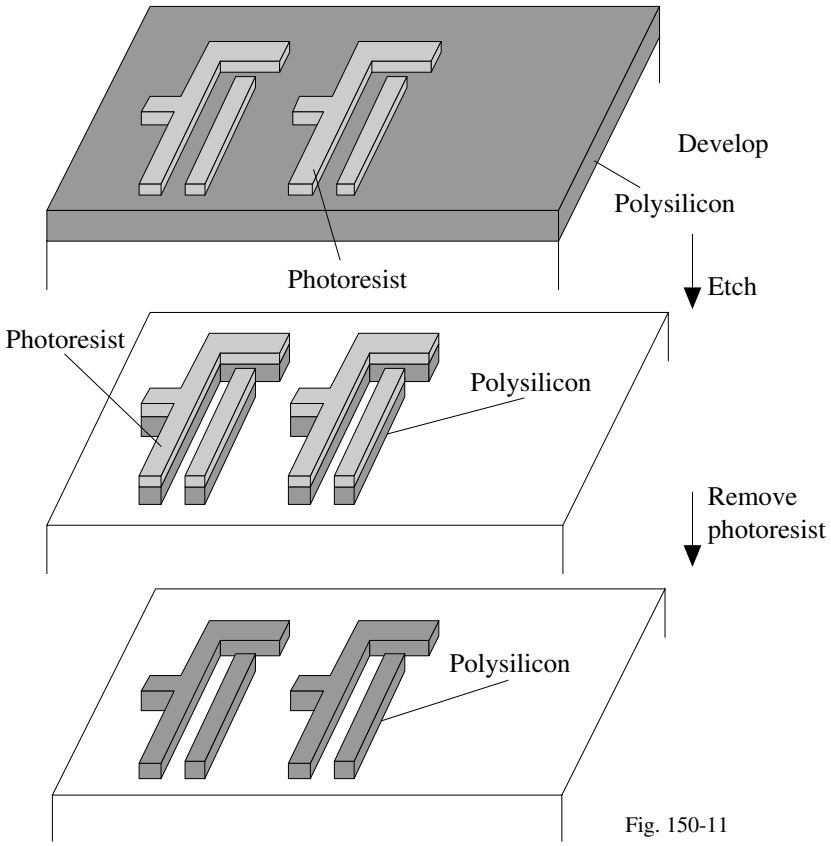


Fig. 150-11

Illustration of Photolithography - Negative Photoresist

(Not used much any more)

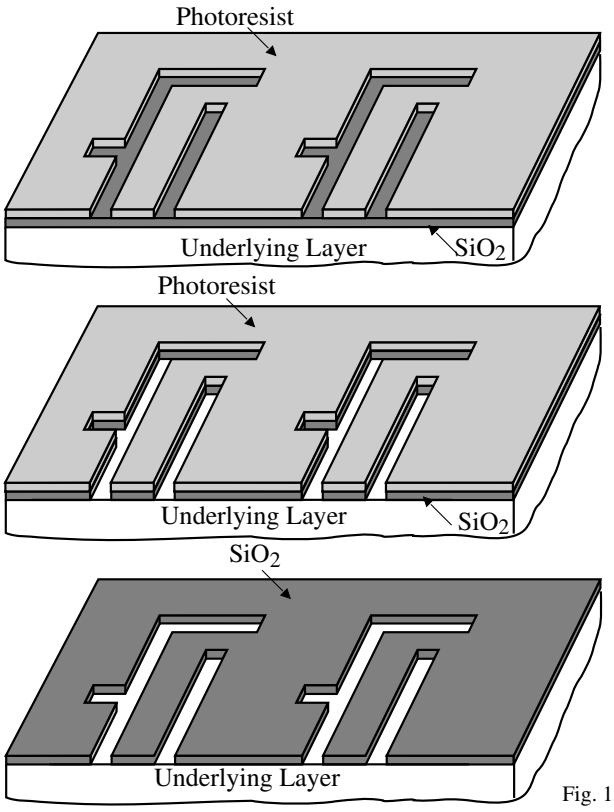


Fig. 150-12

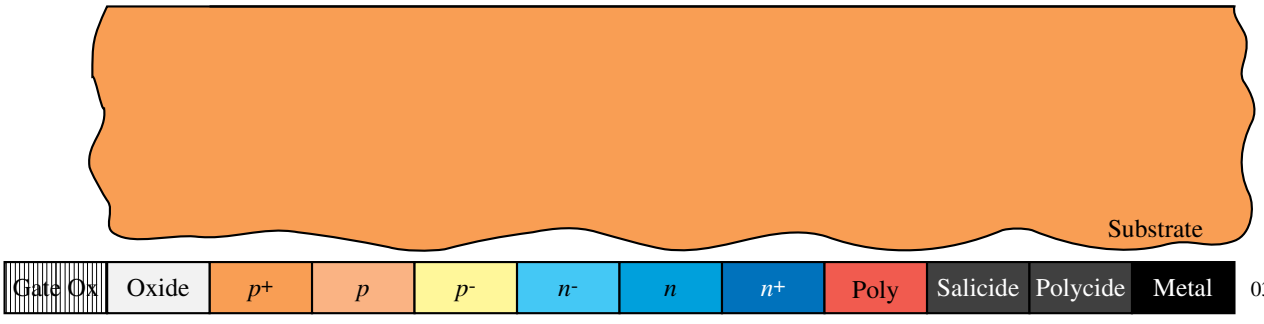
TYPICAL DSM CMOS FABRICATION PROCESS

Major Fabrication Steps for a DSM CMOS Process

1.) *p* and *n* wells
2.) Shallow trench isolation
3.) Threshold shift
4.) Thin oxide and gate polysilicon
5.) Lightly doped drains and sources
6.) Sidewall spacer
7.) Heavily doped drains and sources
8.) Siliciding (Salicide and Polycide)
9.) Bottom metal, tungsten plugs, and oxide
10.) Higher level metals, tungsten plugs/vias, and oxide
11.) Top level metal, vias and protective oxide

Step 1 – Starting Material

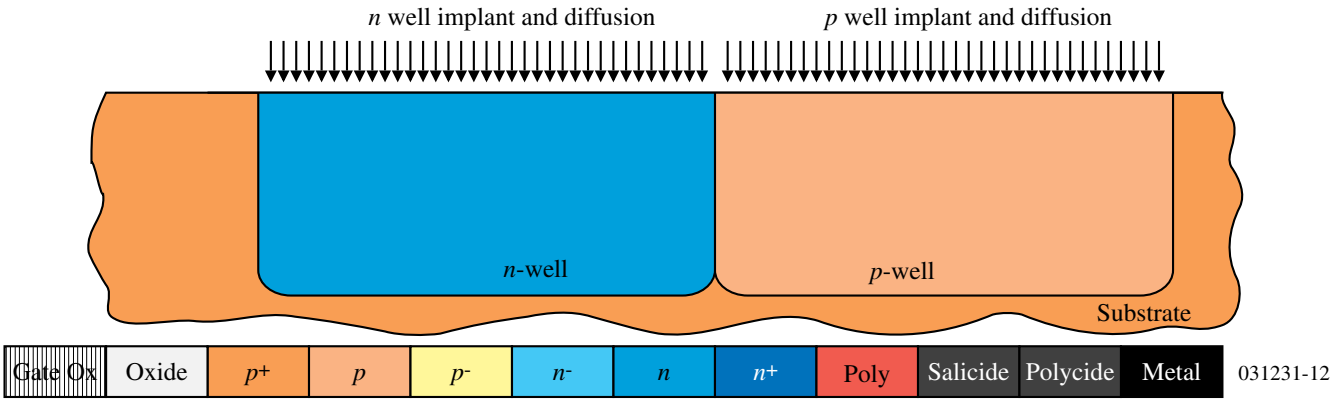
The substrate should be highly doped to act like a good conductor.



Step 2 - *n* and *p* wells

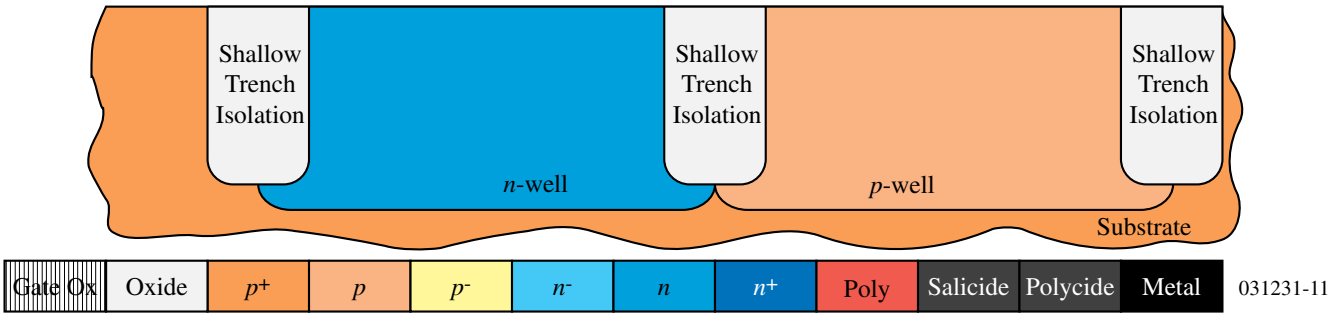
These are the areas where the transistors will be fabricated - NMOS in the *p*-well and PMOS in the *n*-well.

Done by implantation followed by a deep diffusion.



Step 3 – Shallow Trench Isolation

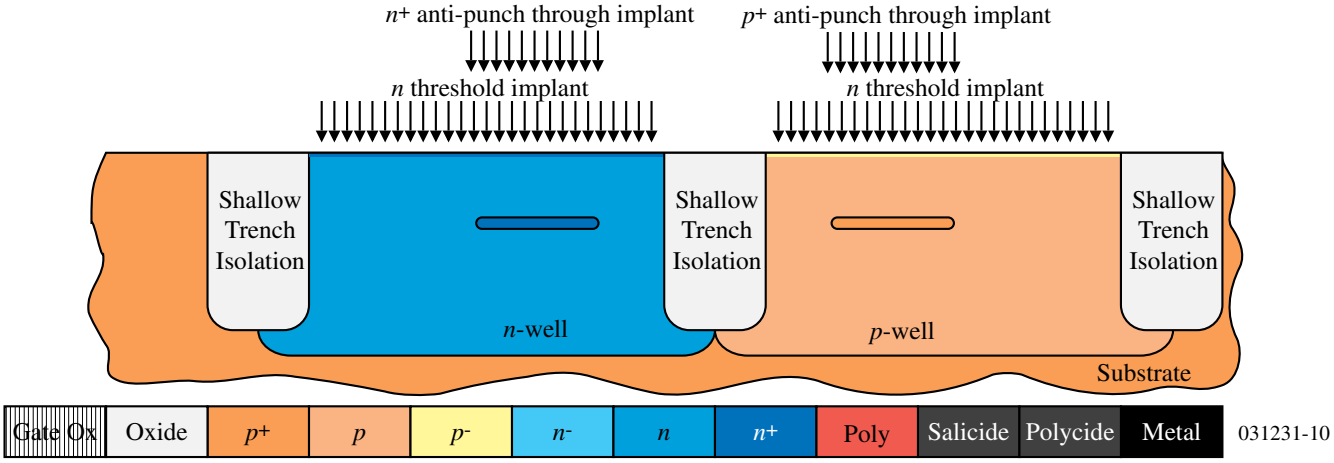
The shallow trench isolation (STI) electrically isolates one region/transistor from another.



Step 4 – Threshold Shift and Anti-Punch Through Implants

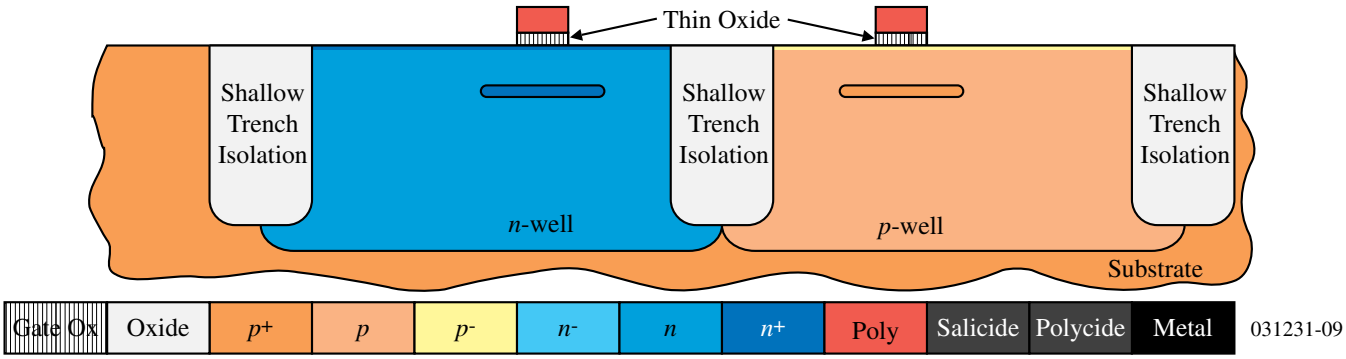
The natural thresholds of the NMOS is about 0V and of the PMOS is about –1.2V. An *n*-implant is used to make the NMOS harder to invert and the PMOS easier resulting in threshold voltages balanced around zero volts.

Also an implant can be applied to create a higher-doped region beneath the channels to prevent punch-through from the drain depletion region extending to source depletion region.



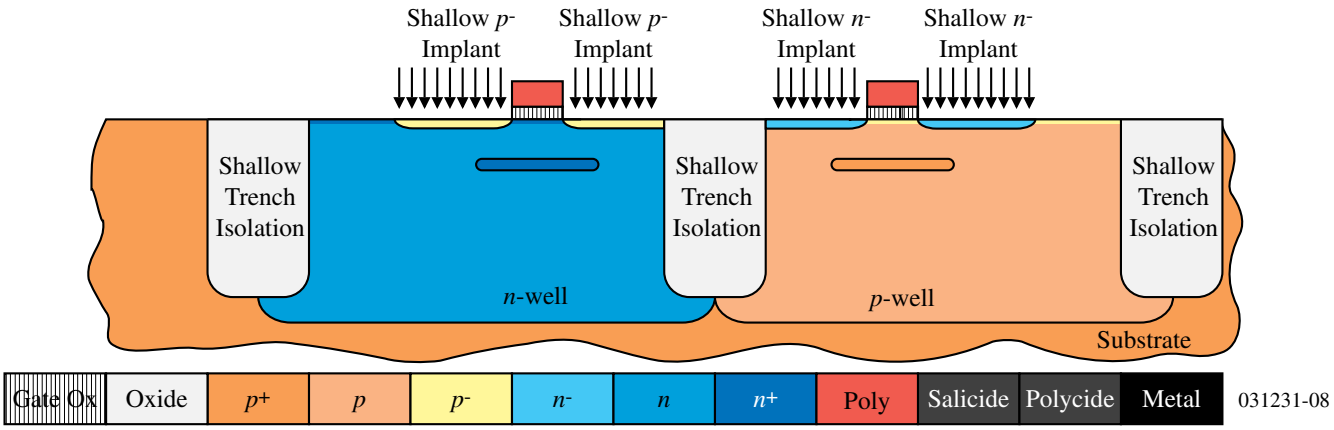
Step 5 – Thin Oxide and Polysilicon Gates

A thin oxide is deposited followed by polysilicon. These layers are removed where they are not wanted.



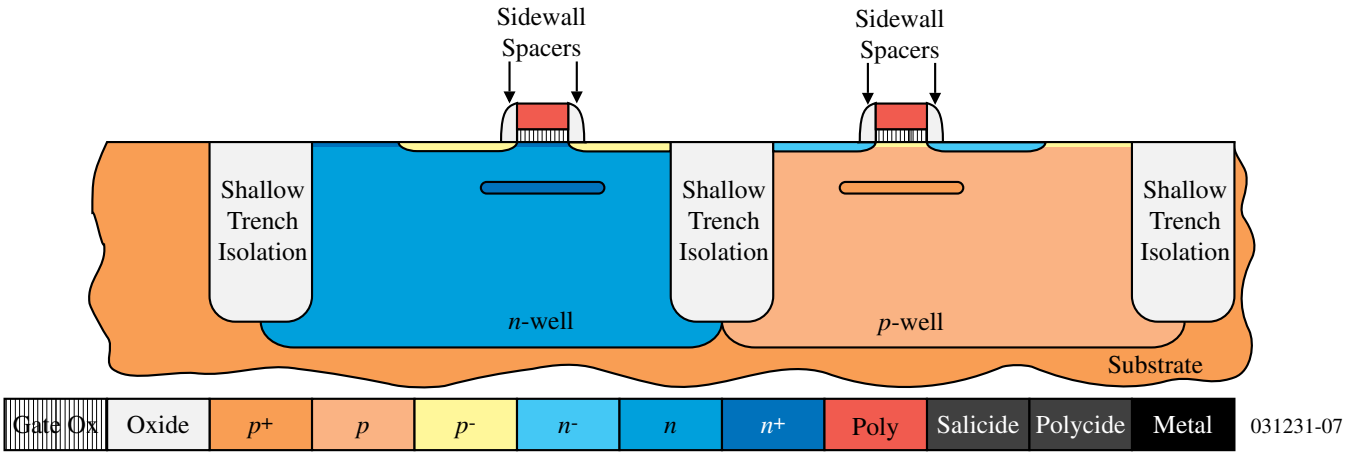
Step 6 – Lightly Doped Drains and Sources

A lightly-doped implant is used to create a lightly-doped source and drain next to the channel of the MOSFETs.



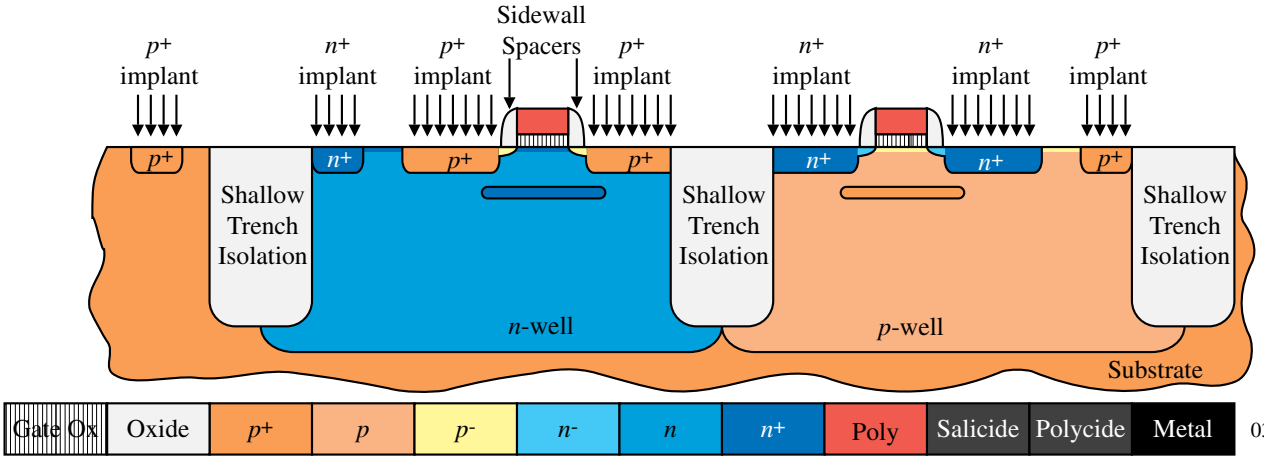
Step 7 – Sidewall Spacers

A layer of dielectric is deposited on the surface and removed in such a way as to leave "sidewall spacers" next to the thin-oxide-polysilicon-polycide sandwich. These sidewall spacers will prevent the part of the source and drain next to the channel from becoming heavily doped.



Step 8 – Implantation of the Heavily Doped Sources and Drains

Note that not only does this step provide the completed sources and drains but allows for ohmic contact into the wells and substrate.



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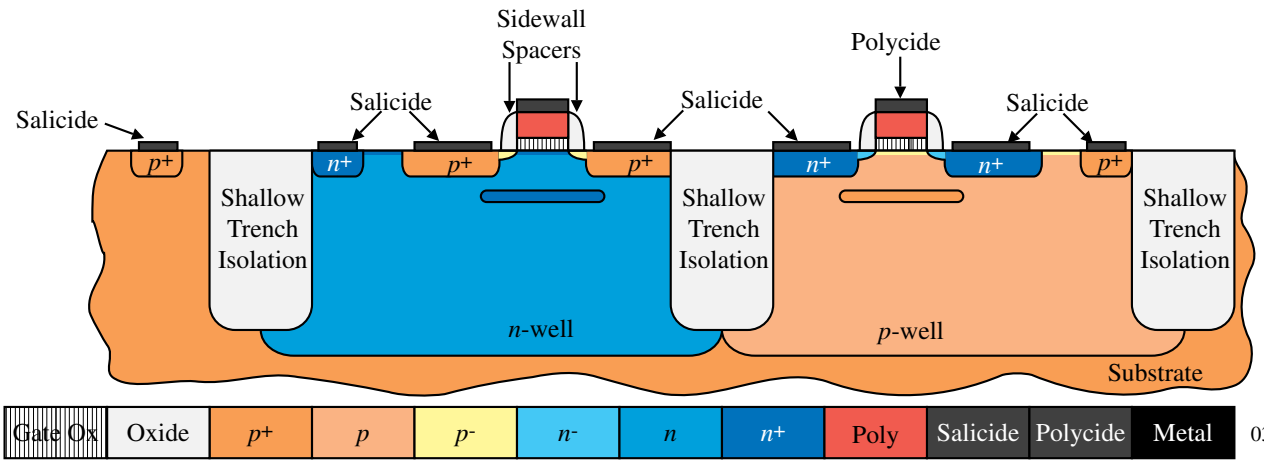
Step 9 – Siliciding

Siliciding and polyciding is used to reduce interconnect resistivity by placing a low-resistance silicide such as $TiSi_2$, WSi_2, $TaSi_2$, etc. on top of the diffusions.



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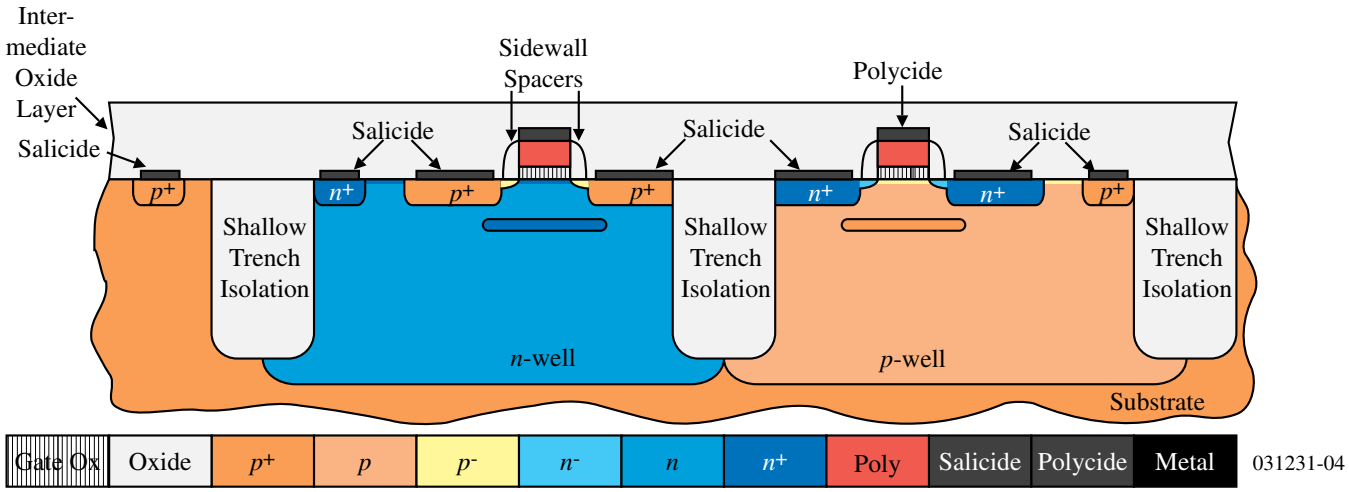
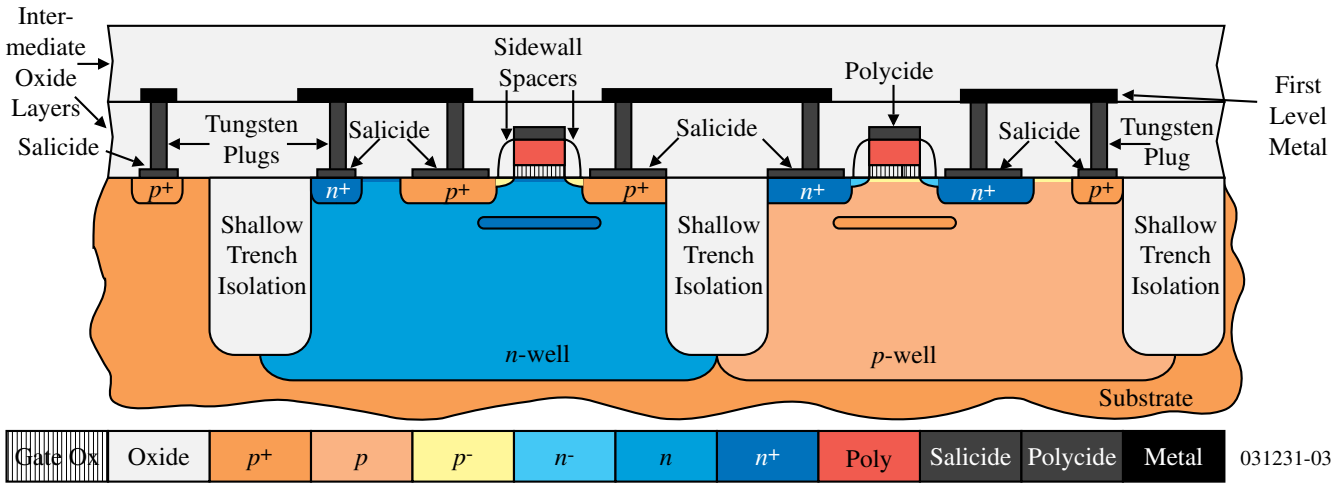
Step 10 – Intermediate Oxide Layer

An oxide layer is used to cover the transistors and to planarize the surface.



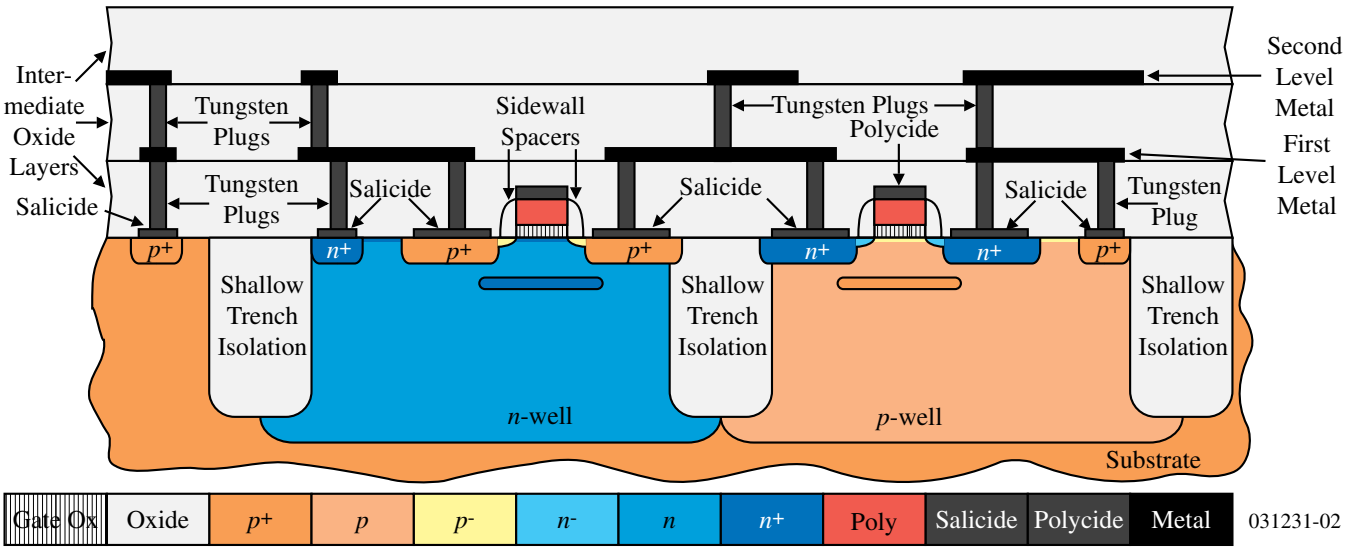
Step 11- First-Level Metal

Tungsten plugs are built through the lower intermediate oxide layer to provide contact between the devices, wells and substrate to the first-level metal.



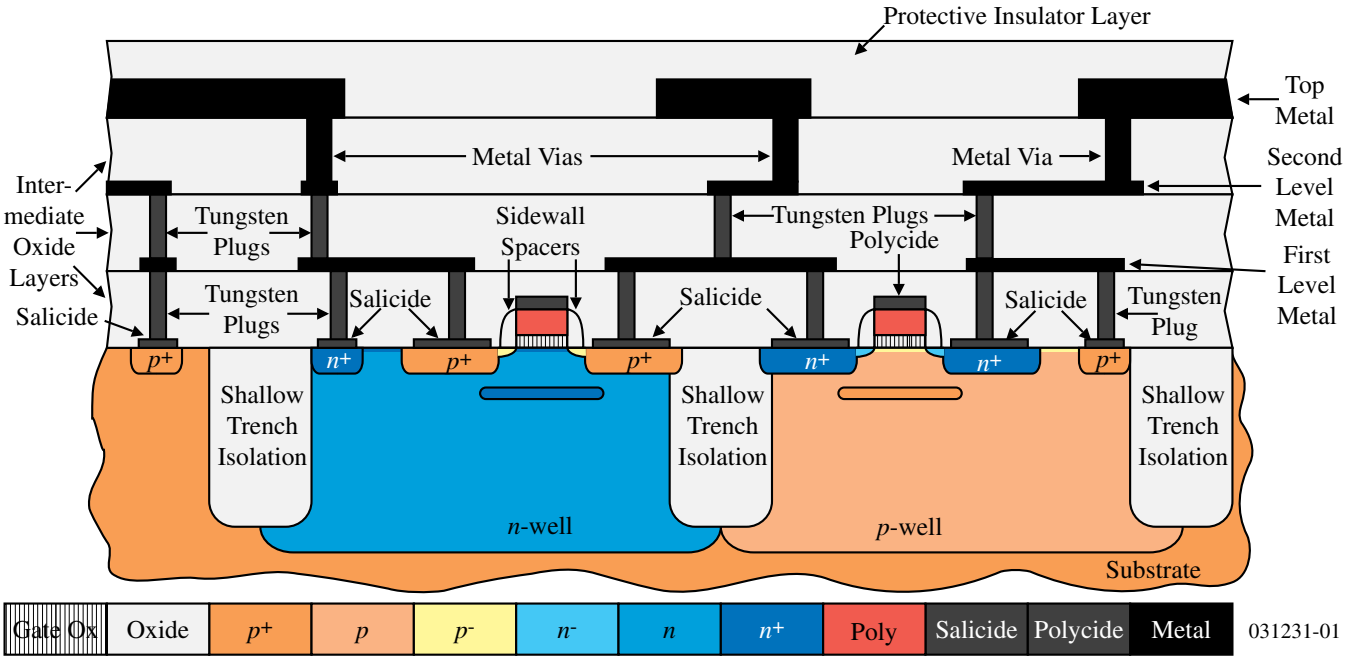
Step 12 – Second-Level Metal

The previous step is repeated to from the second-level metal.



Completed Fabrication

After multiple levels of metal are applied, the fabrication is completed with a thicker top-level metal and a protective layer to hermetically seal the circuit from the environment. Note that metal is used for the upper level metal vias. The chip is electrically connected by removing the protective layer over large bonding pads.



Scanning Electron Microscope of a MOSFET Cross-section

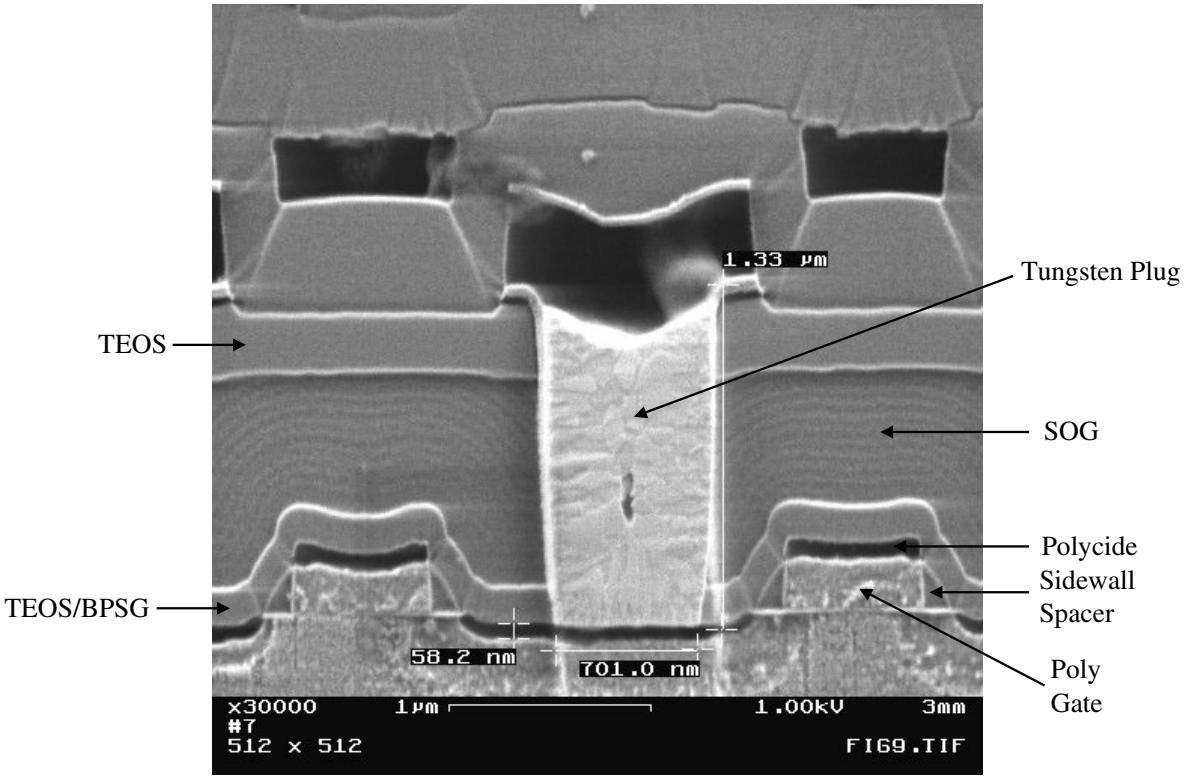


Fig. 2.8-20

Scanning Electron Microscope Showing Metal Levels and Interconnect

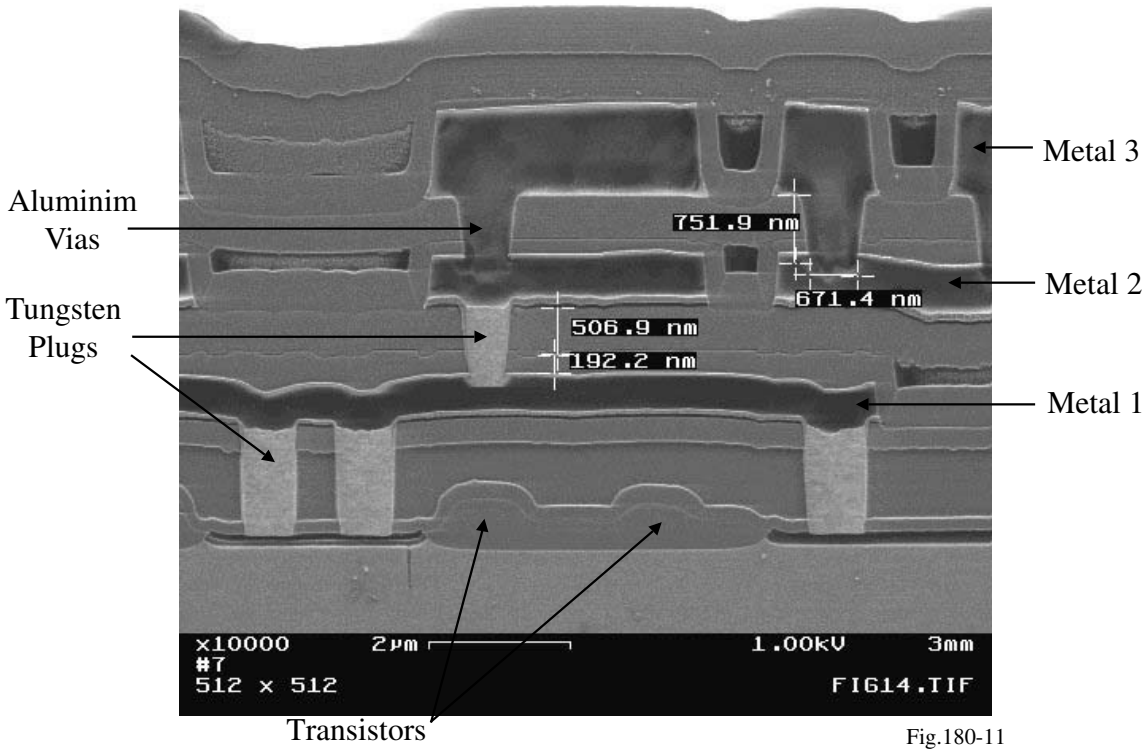


Fig.180-11

SUMMARY

- Fabrication is the means by which the circuit components, both active and passive, are built as an integrated circuit.
- Basic process steps include:

  1.) Oxide growth 2.) Thermal diffusion 3.) Ion implantation
  4.) Deposition 5.) Etching 6.) Epitaxy
- The complexity of a process can be measured in the terms of the number of masking steps or masks required to implement the process.
- Major Processing Steps for DSM CMOS:

  1.) *p* and *n* wells
  2.) Shallow trench isolation
  3.) Threshold shift
  4.) Thin oxide and gate polysilicon
  5.) Lightly doped drains and sources
  6.) Sidewall spacer
  7.) Heavily doped drains and sources
  8.) Siliciding (Salicide and Polycide)
  9.) Bottom metal, tungsten plugs, and oxide
  10.) Higher level metals, tungsten plugs/vias, and oxide
  11.) Top level metal, vias and protective oxide

INTEGRATED CIRCUIT LAYOUT

MOS Transistor Layout

Example of the layout of a single MOS transistor:

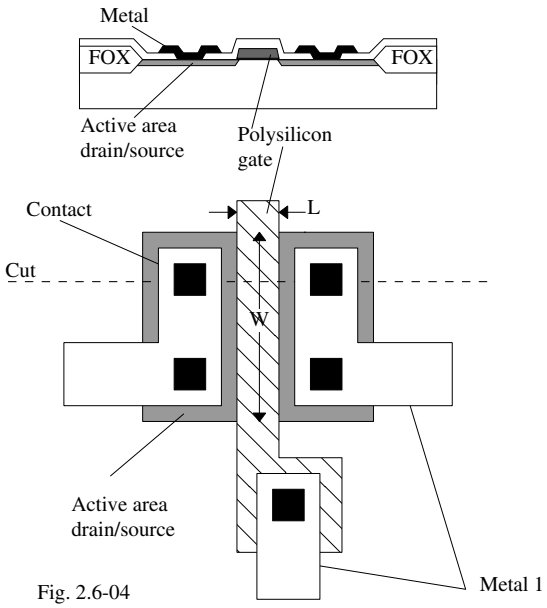


Fig. 2.6-04

Comments:

- Make sure to contact the source and drain with multiple contacts to evenly distribute the current flow under the gate.
- Minimize the area of the source and drain to reduce bulk-source/drain capacitance.

Resistor Layout

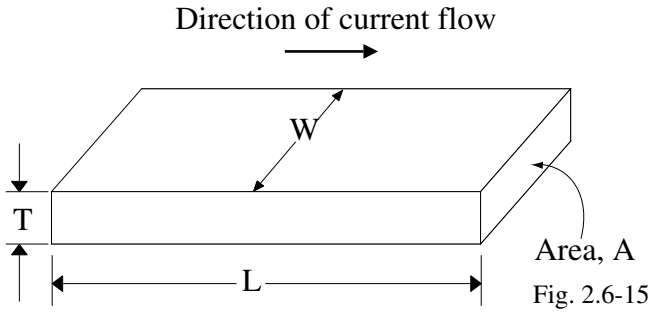


Fig. 2.6-15

Resistance of a conductive sheet is expressed in terms of

$$R = \frac{\rho L}{A} = \frac{\rho L}{WT} \ (\Omega)$$

where

ρ = resistivity in Ω-m

Ohms/square:

$$R = \left(\frac{\rho}{T}\right)\frac{L}{W} = \rho_S \frac{L}{W} \ (\Omega)$$

where

ρ_S is a sheet resistivity and has the units of ohms/square

Example of Resistor Layouts

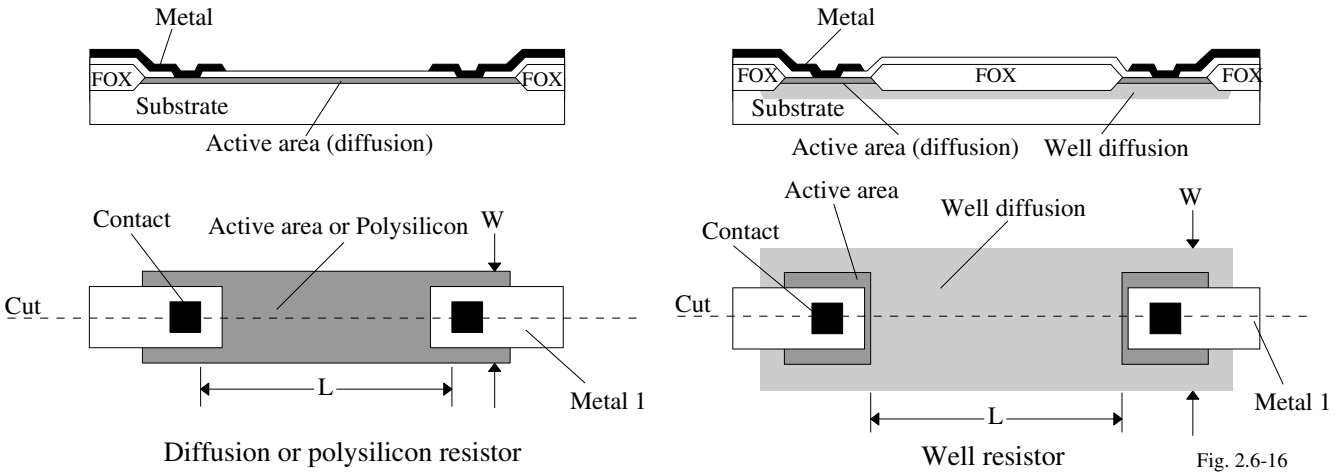


Fig. 2.6-16

Corner corrections:

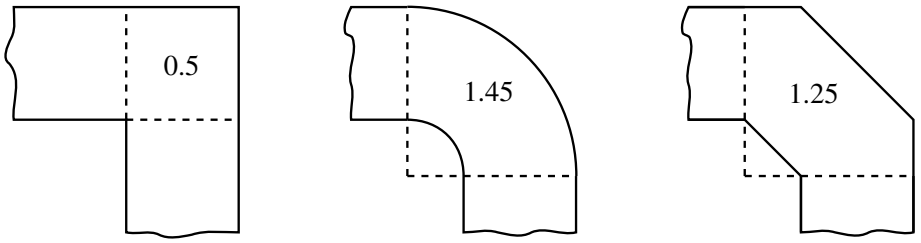


Fig. 2.6-16B

Example 1 - Resistance Calculation

Given a polysilicon resistor like that drawn above with W=0.8μm and L=20μm, calculate ρ_S (in Ω/❑), the number of squares of resistance, and the resistance value. Assume that ρ for polysilicon is 9×10^{-4} Ω-cm and polysilicon is 3000 Å thick. Ignore any contact resistance.

Solution

First calculate ρ_S.

$$\rho_S = \frac{\rho}{T} = \frac{9 \times 10\text{-}4\ \Omega\text{-cm}}{3000 \times 10\text{-}8\ \text{cm}} = 30\ \Omega/❑$$

The number of squares of resistance, N, is

$$N = \frac{L}{W} = \frac{20\mu\text{m}}{0.8\mu\text{m}} = 25$$

giving the total resistance as

$$R = \rho_S \times N = 30 \times 25 = 750\ \Omega$$

Design Rules

Design rules are geometrical constraints that guarantee the proper operation of a circuit implemented by a given CMOS process.

These rules are necessary to avoid problems such as device misalignment, metal fracturing, lack of continuity, etc.

Design rules are expressed in terms of minimum dimensions such as minimum values of:

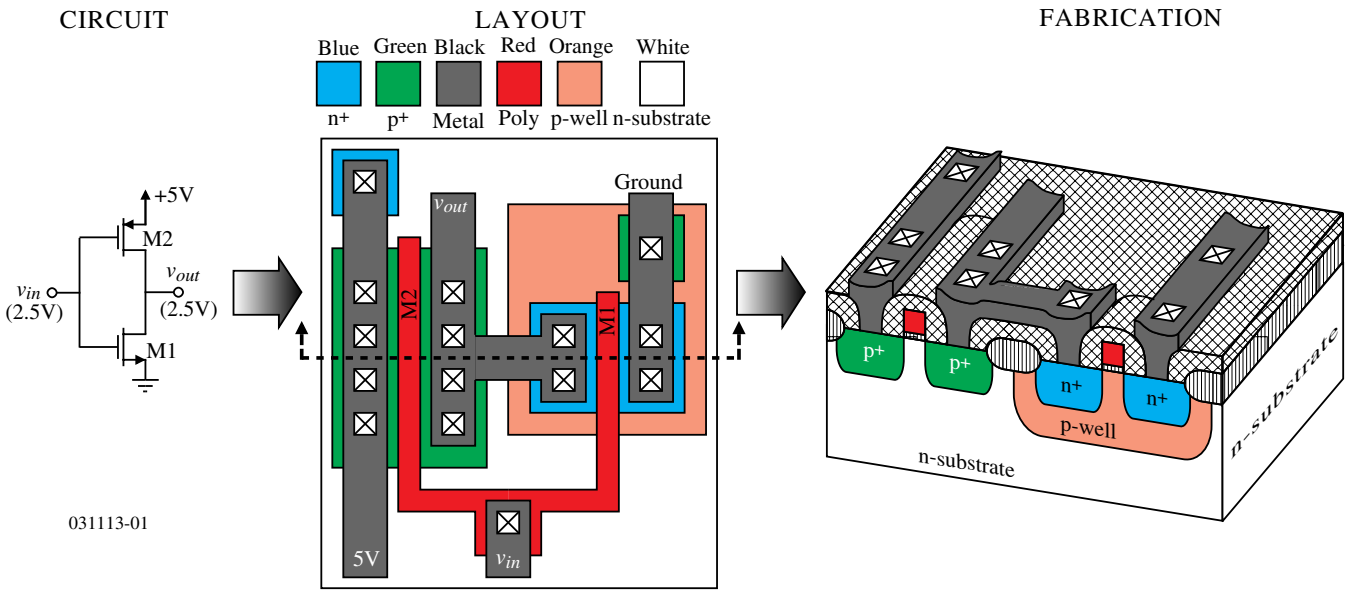
- Widths
- Separations
- Extensions
- Overlaps

• Design rules typically use a minimum feature dimension called “lambda”. Lambda is usually equal to the minimum channel length.

• Minimum resolution of the design rules is typically half lambda.

• In most processes, lambda can be scaled or reduced as the process matures.

Example of the Physical Design Process



BiCMOS TECHNOLOGY

Typical 0.5µm BiCMOS Technology

Masking Sequence:

1. Buried n+ layer
2. Buried p+ layer
3. Collector tub
4. Active area
5. Collector sinker
6. n-well
7. p-well
8. Emitter window
9. Base oxide/implant
10. Emitter implant
11. Poly 1
12. NMOS lightly doped drain
13. PMOS lightly doped drain
14. n+ source/drain
15. p+ source/drain
16. Silicide protection
17. Contacts
18. Metal 1
19. Via 1
20. Metal 2
21. Via 2
22. Metal 3
23. Nitride passivation

Notation:

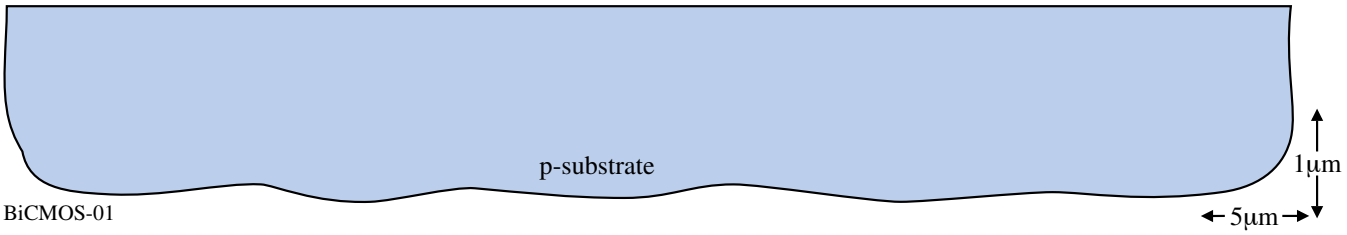
BSPG = Boron and Phosphorus doped Silicate Glass (oxide)

Kooi Nitride = A thin layer of silicon nitride on the silicon surface as a result of the reaction of silicon with the HN3 generated, during the field oxidation.

TEOS = Tetro-Ethyl-Ortho-Silicate. A chemical compound used to deposit conformal oxide films.

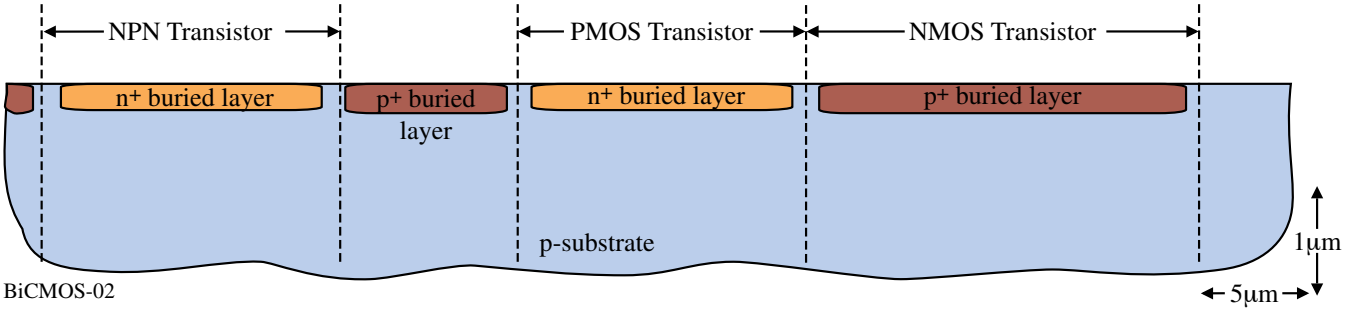
n+ and p+ Buried Layers

Starting Substrate:



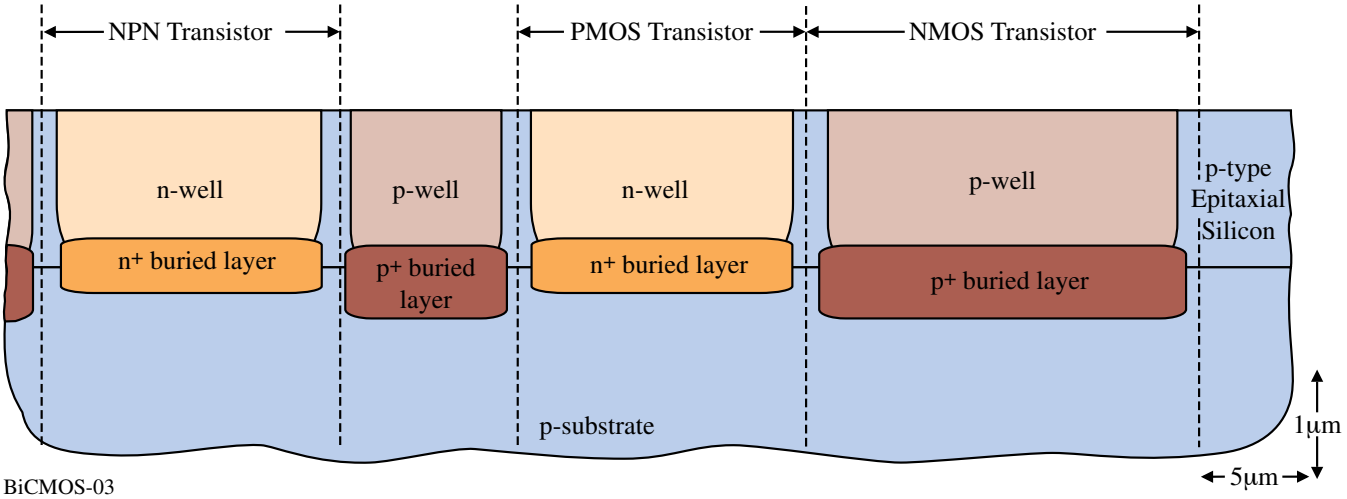
BiCMOS-01

n+ and p+ Buried Layers:



BiCMOS-02

Epitaxial Growth

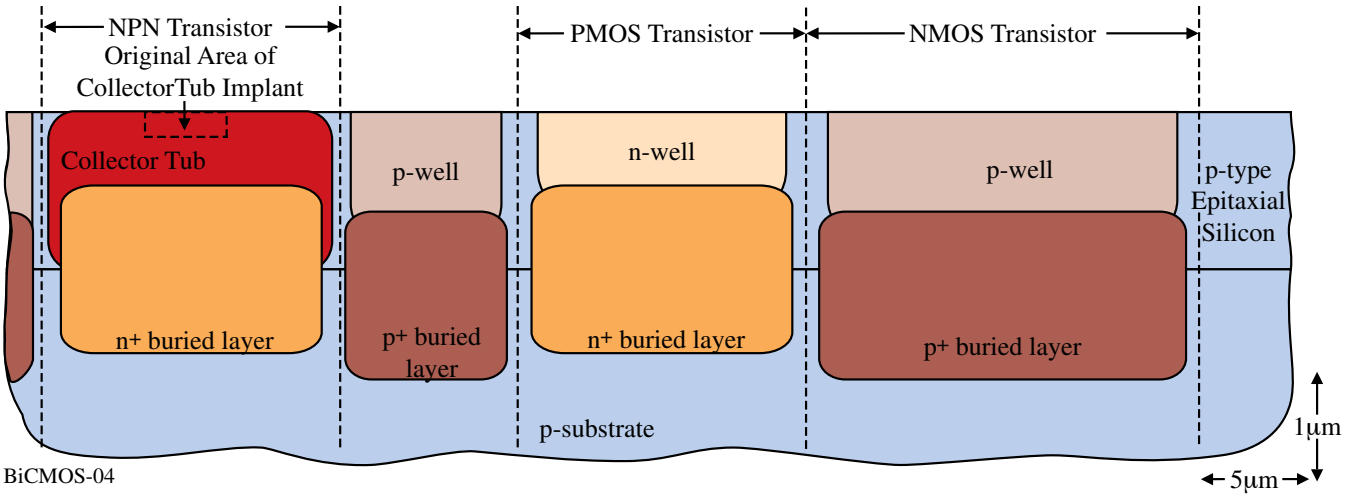


BiCMOS-03

Comment:

- As the epi layer grows vertically, it assumes the doping level of the substrate beneath it.
- In addition, the high temperature of the epitaxial process causes the buried layers to diffuse upward and downward.

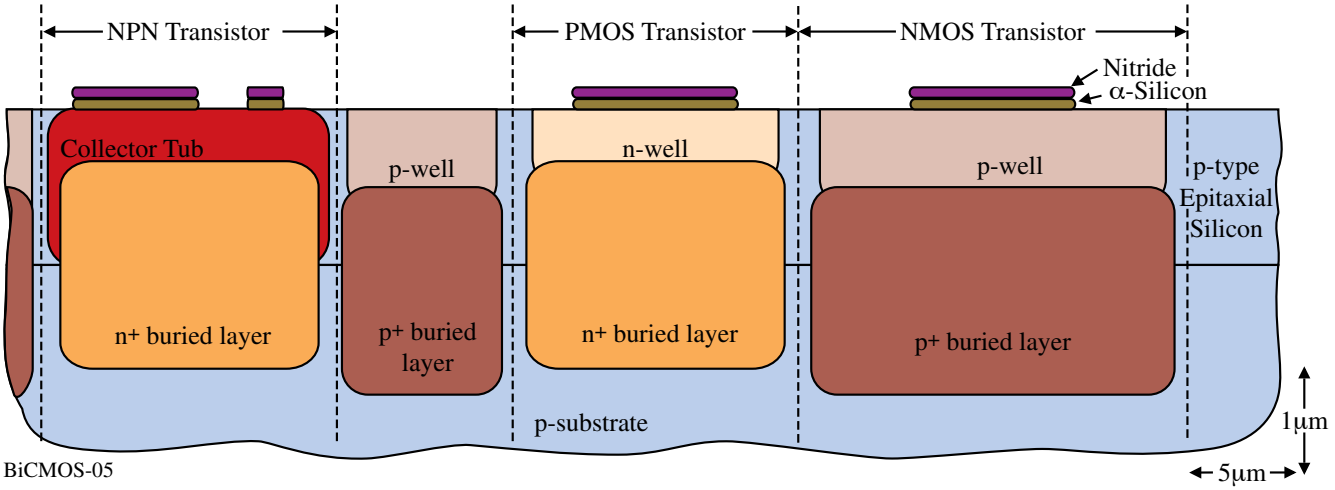
Collector Tub



Comment:

- The collector area is developed by an initial implant followed by a drive-in diffusion to form the collector tub.

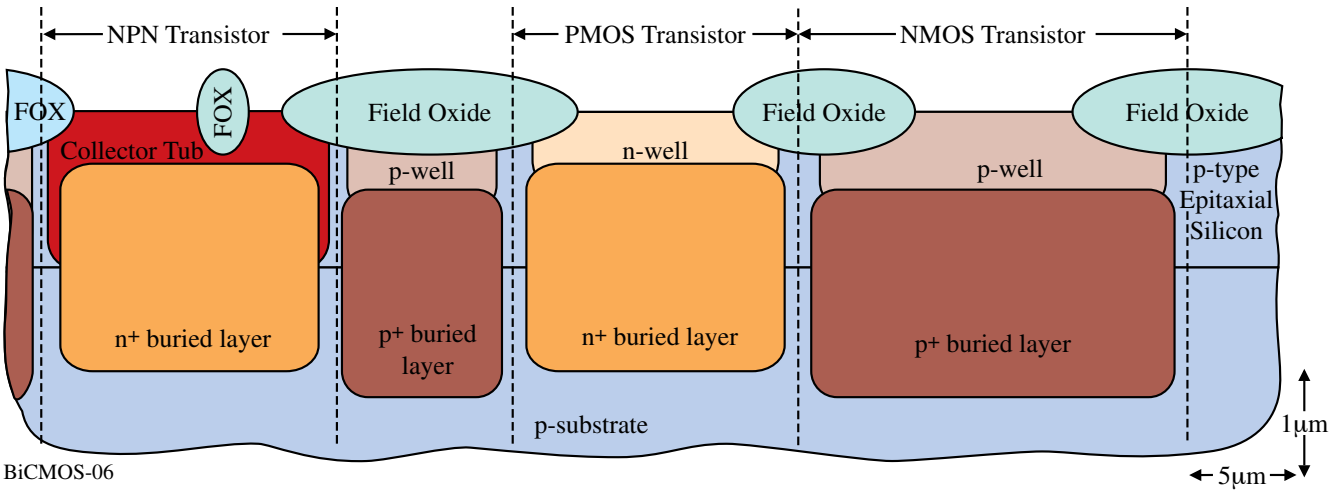
Active Area Definition



Comment:

- The silicon nitride is use to impede the growth of the thick oxide which allows contact to the substrate
- α-silicon is used for stress relief and to minimize the bird's beak encroachment

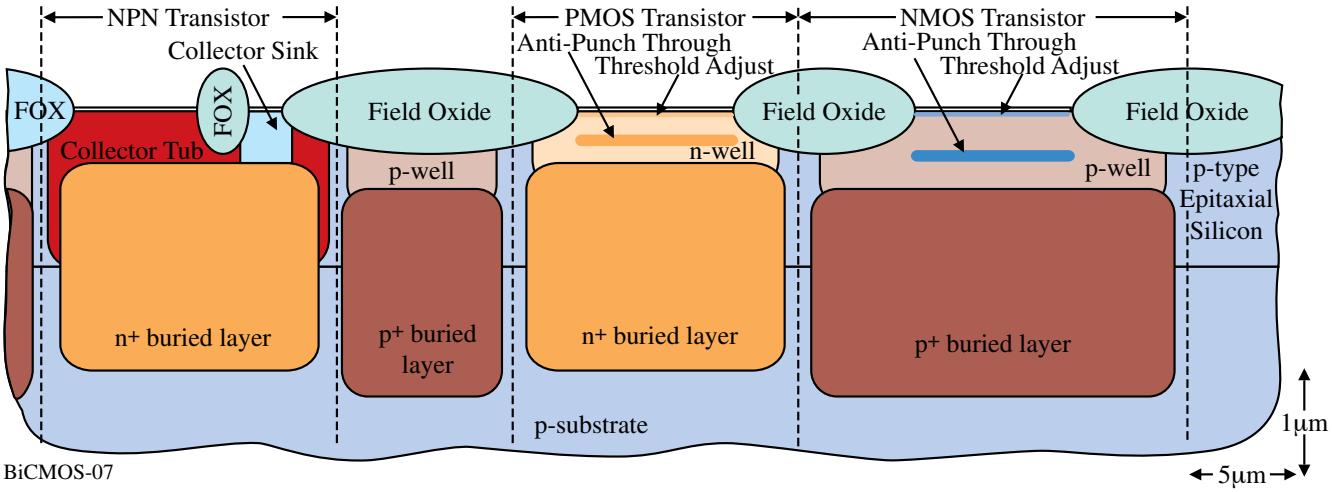
Field Oxide



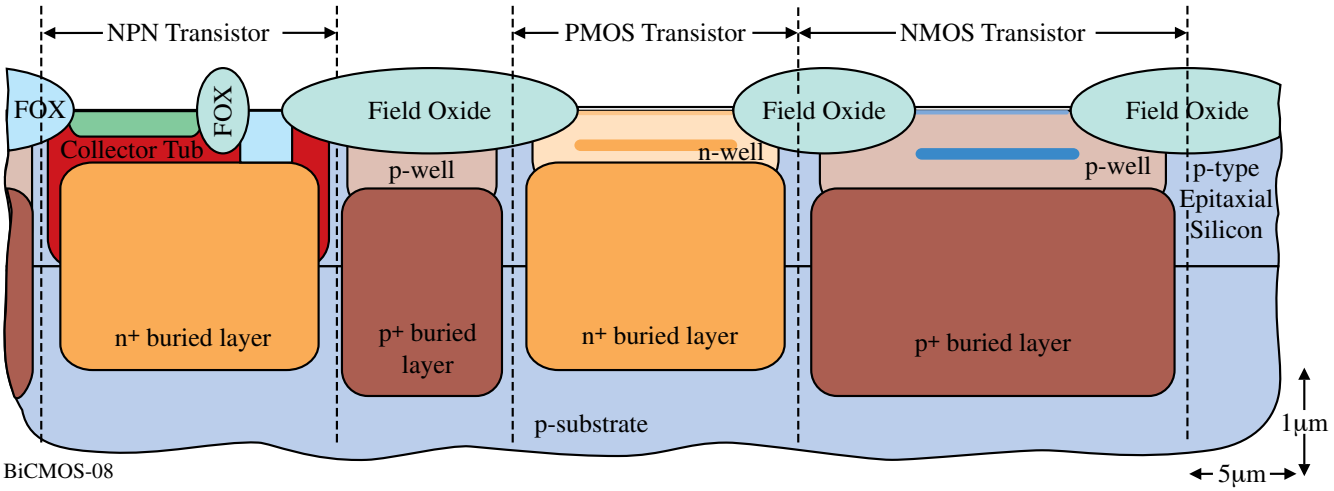
Comments:

- The field oxide is used to isolate surface structures (i.e. metal) from the substrate

Collector Sink and n-Well and p-Well Definitions

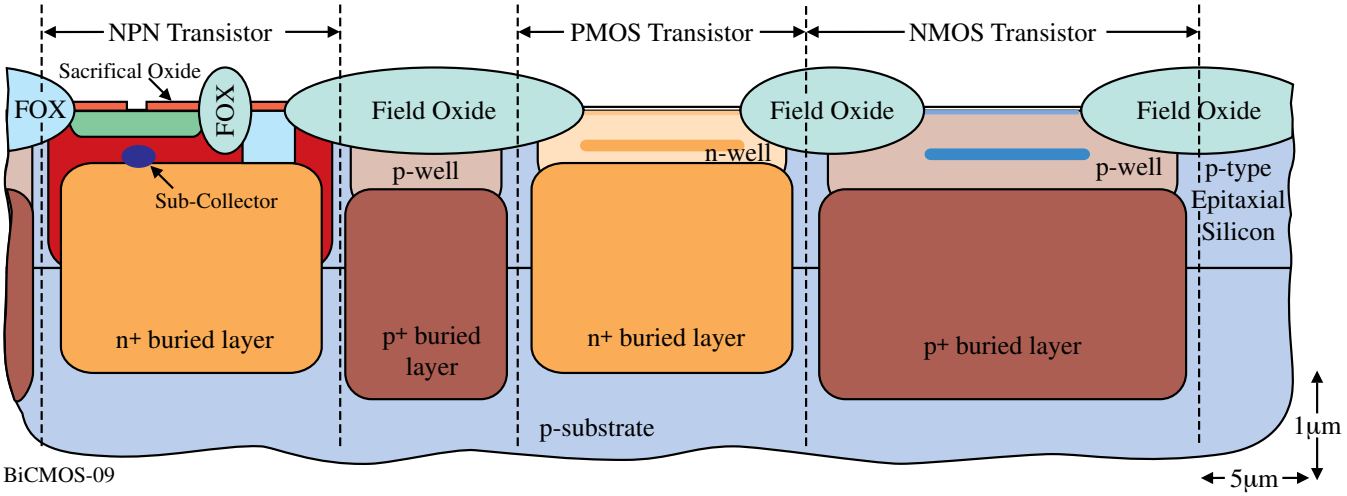


Base Definition



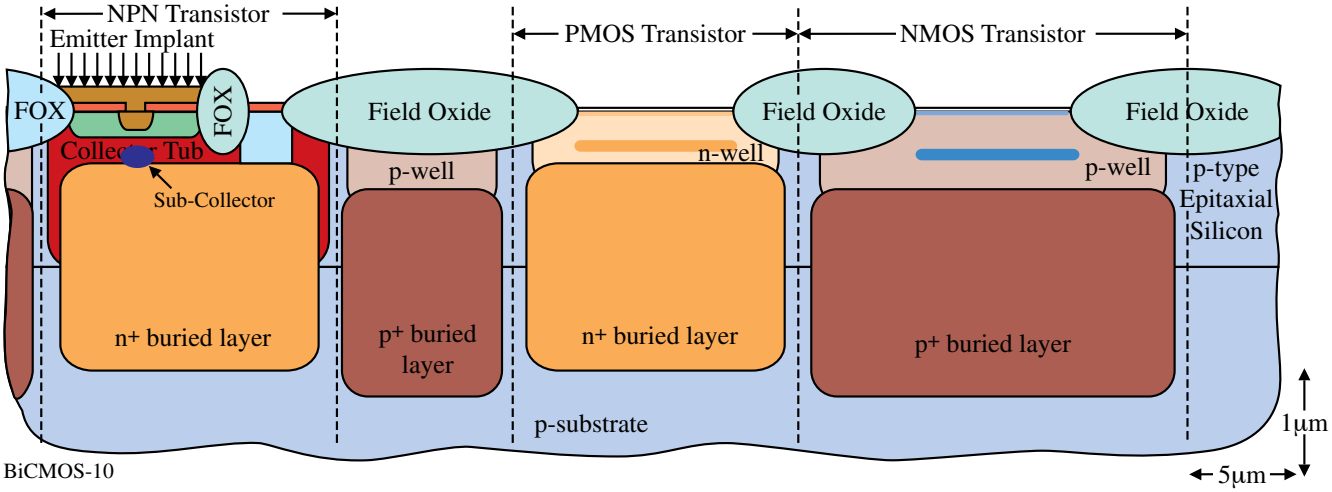
BiCMOS-08

Definition of the Emitter Window and Sub-Collector Implant



BiCMOS-09

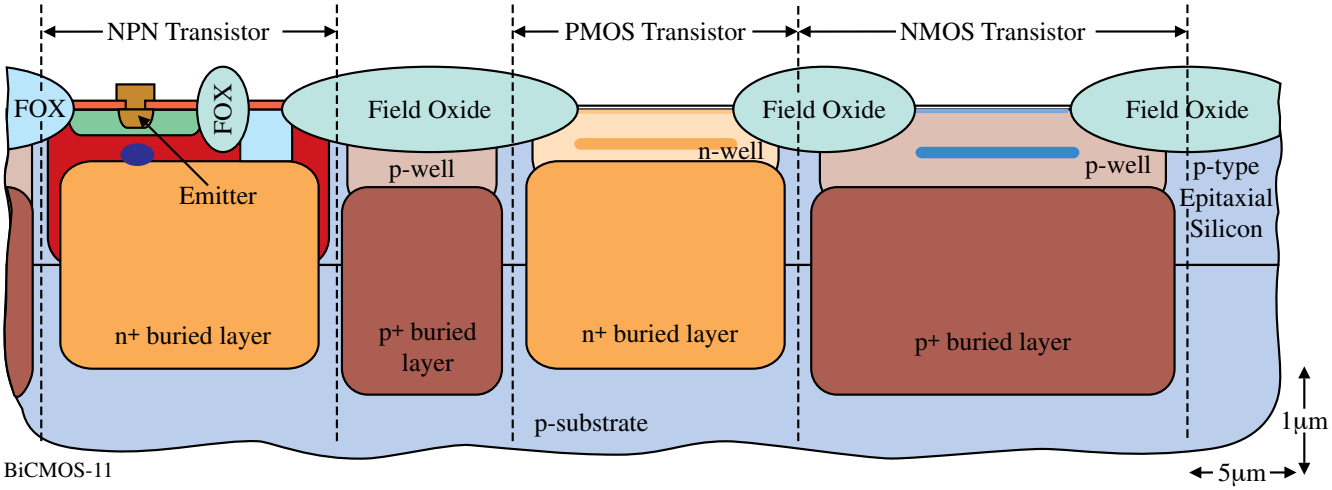
Emitter Implant



Comments:

- The polysilicon above the base is implanted with n-type carriers

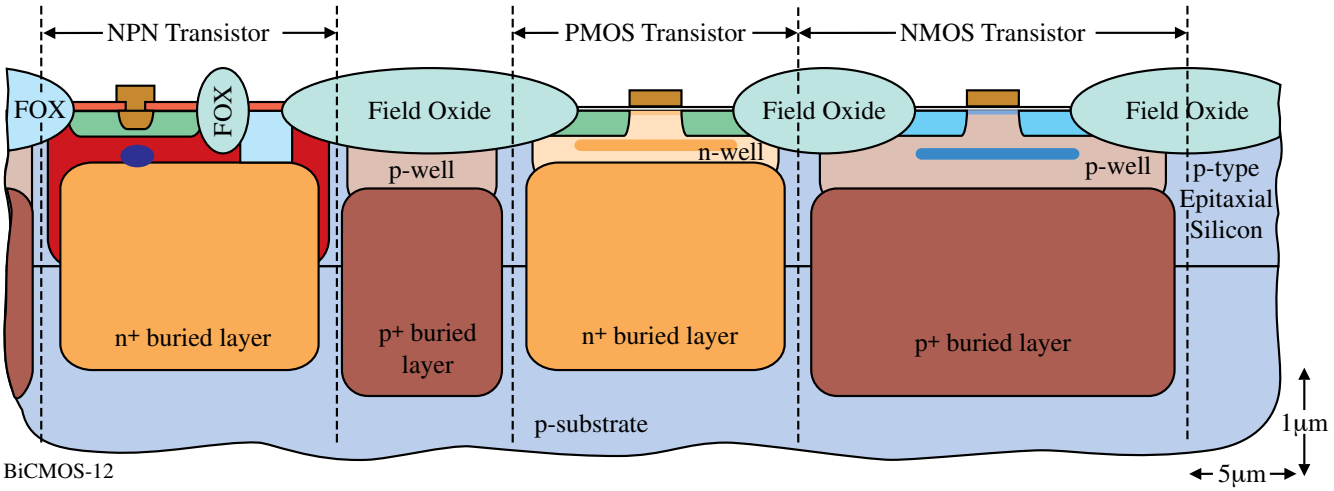
Emitter Diffusion



Comments:

- The polysilicon not over the emitter window is removed and the n-type carriers diffuse into the base forming the emitter

Formation of the MOS Gates and LD Drains/Sources

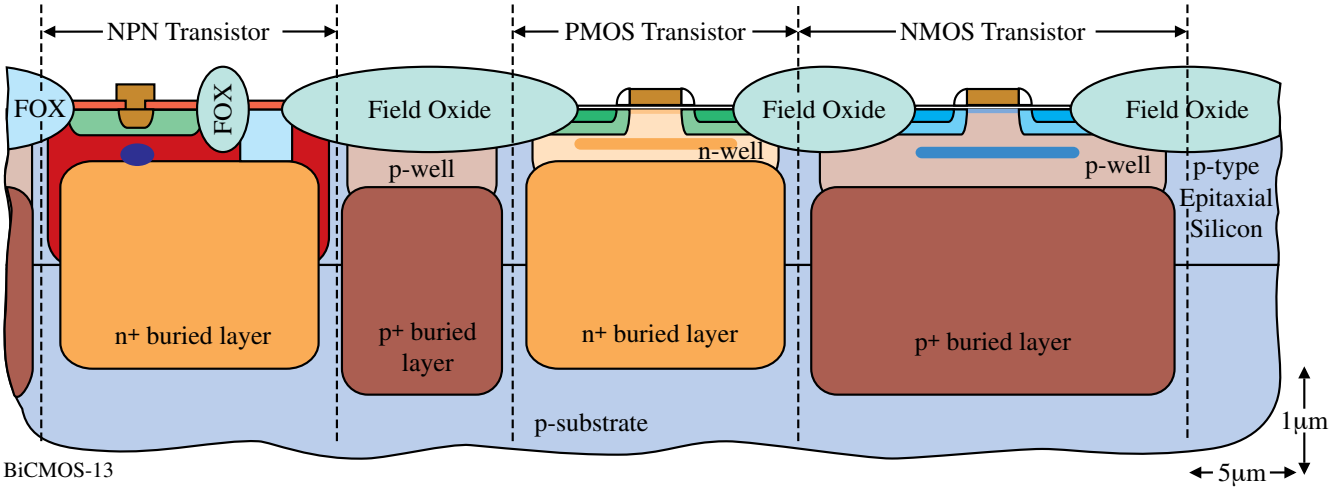


BiCMOS-12

Comments:

- The surface of the region where the MOSFETs are to be built is cleared and a thin gate oxide is deposited with a polysilicon layer on top of the thin oxide
- The polysilicon is removed over the source and drain areas
- A light source/drain diffusion is done for the NMOS and PMOS (separately)

Heavily Doped Source/Drain

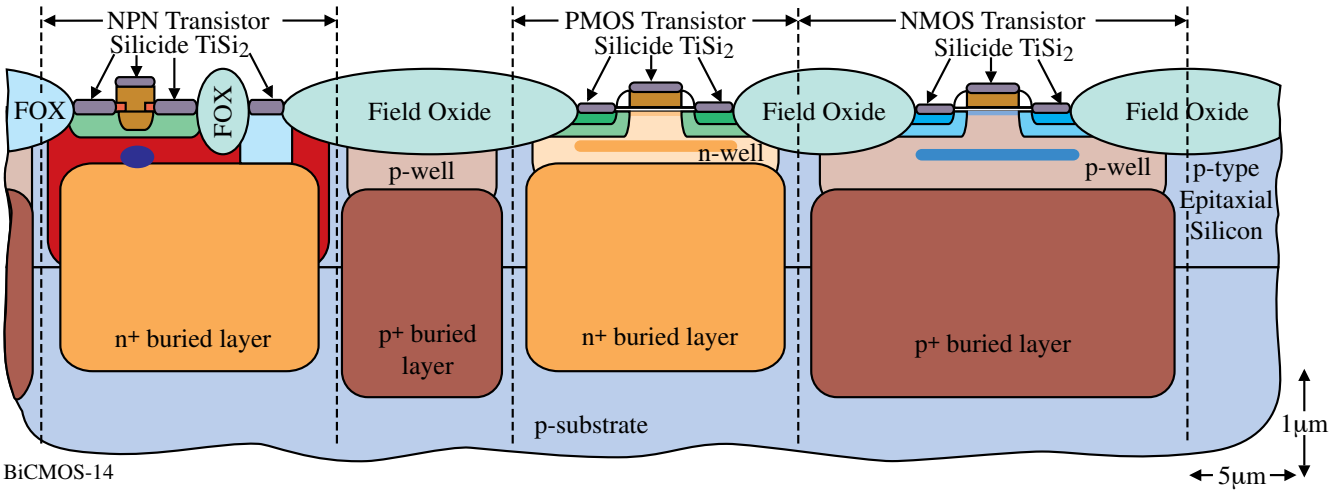


BiCMOS-13

Comments:

- The sidewall spacers prevent the heavy source/drain doping from being near the channel of the MOSFET

Siliciding

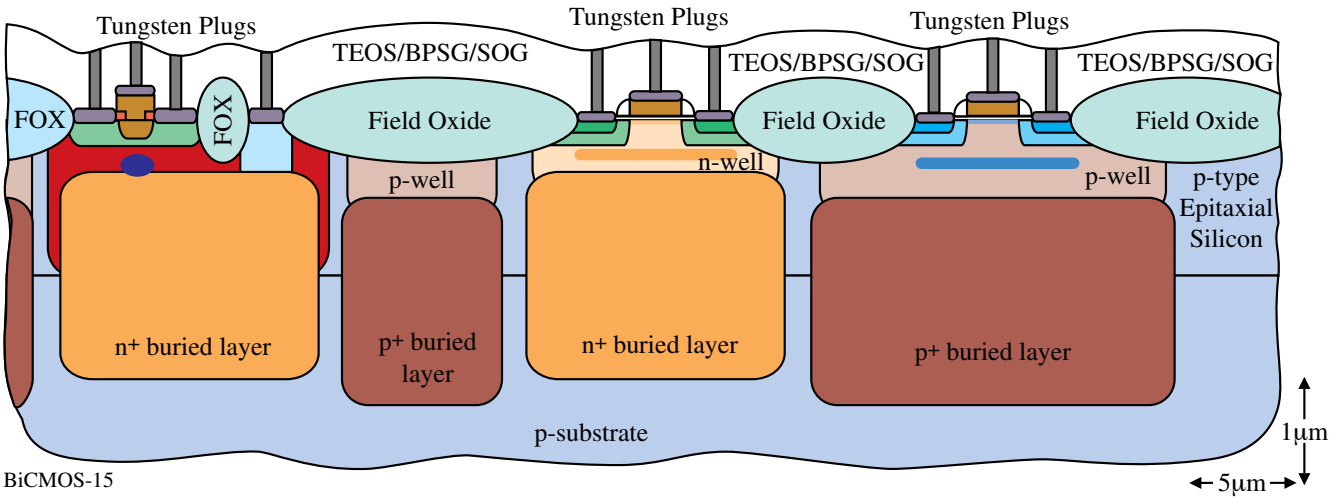


BiCMOS-14

Comments:

- Siliciding is used to reduce the resistance of the polysilicon and to provide ohmic contacts to the base, emitter, collector, sources and drains

Contacts

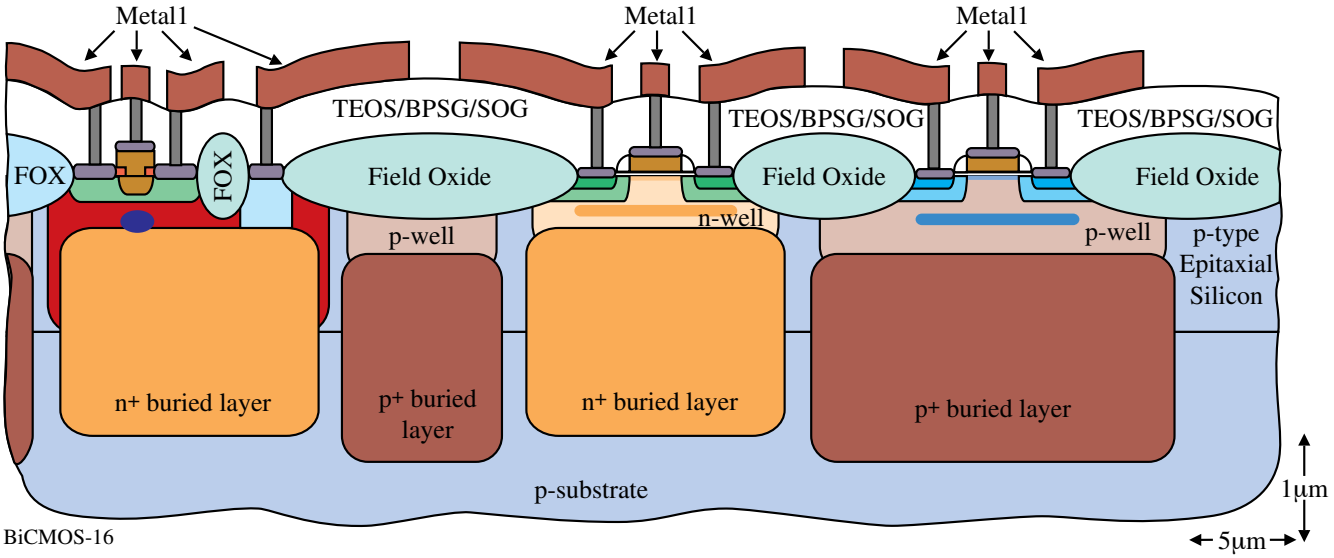


BiCMOS-15

Comments:

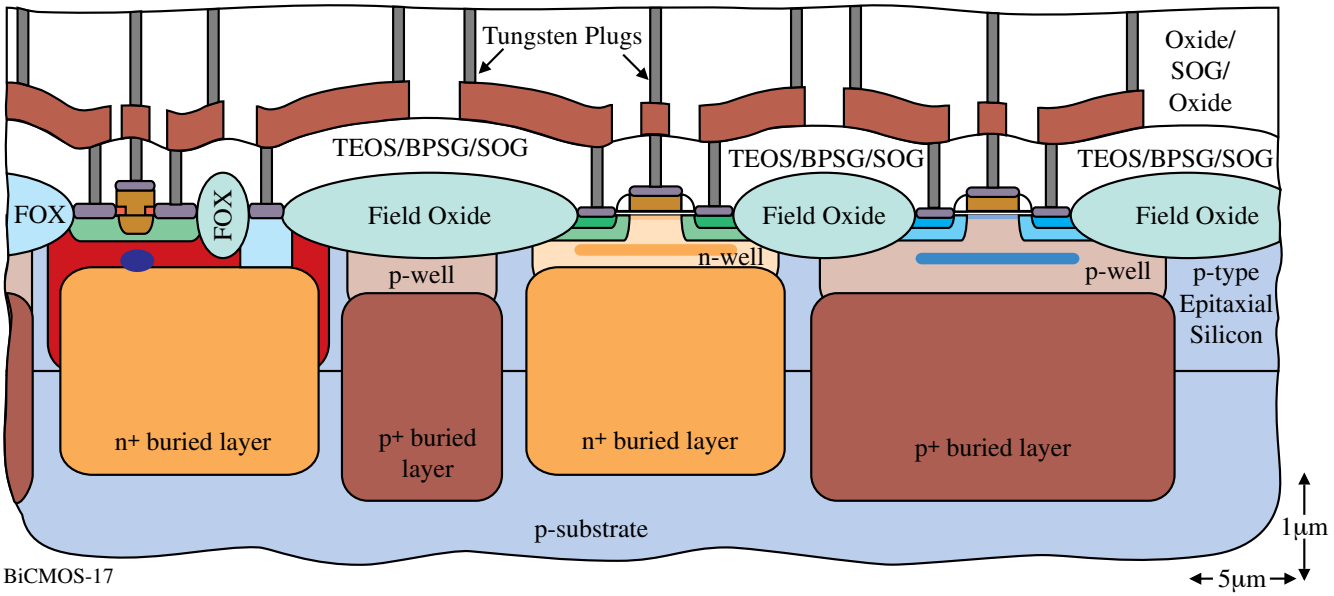
- A dielectric is deposited over the entire wafer
- One of the purposes of the dielectric is to smooth out the surface
- Tungsten plugs are used to make electrical contact between the transistors and metal1

Metal1



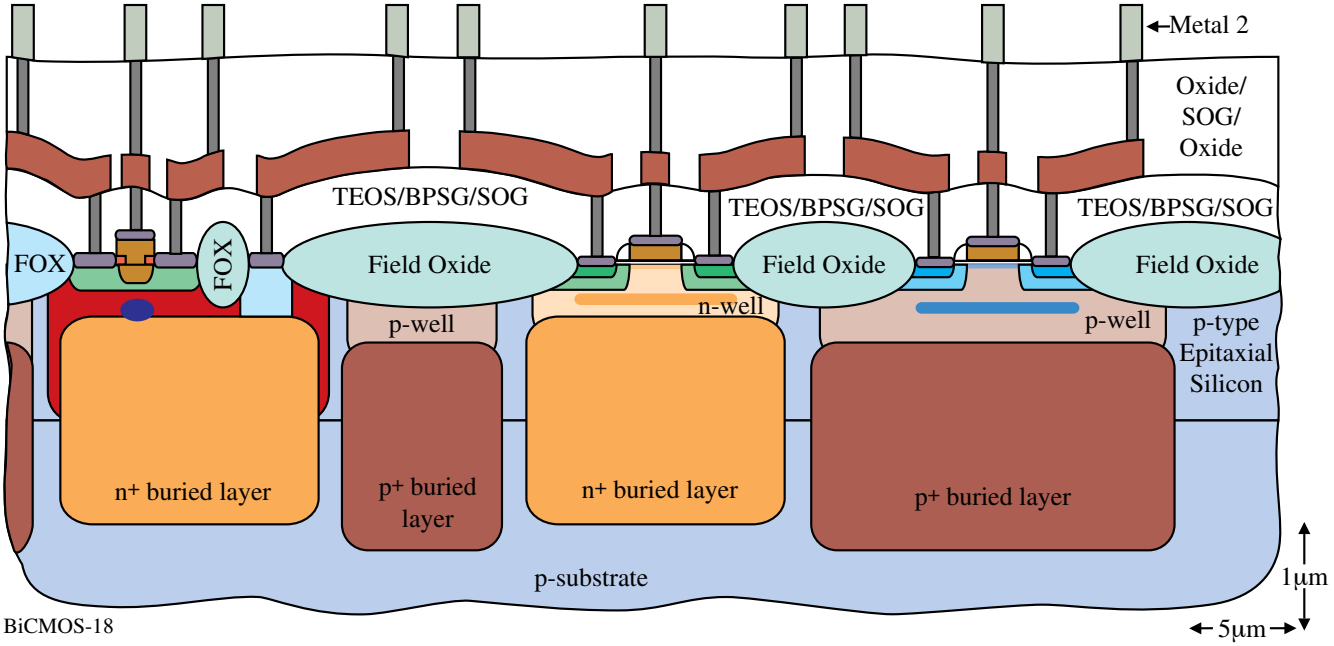
BiCMOS-16

Metal1-Metal2 Vias



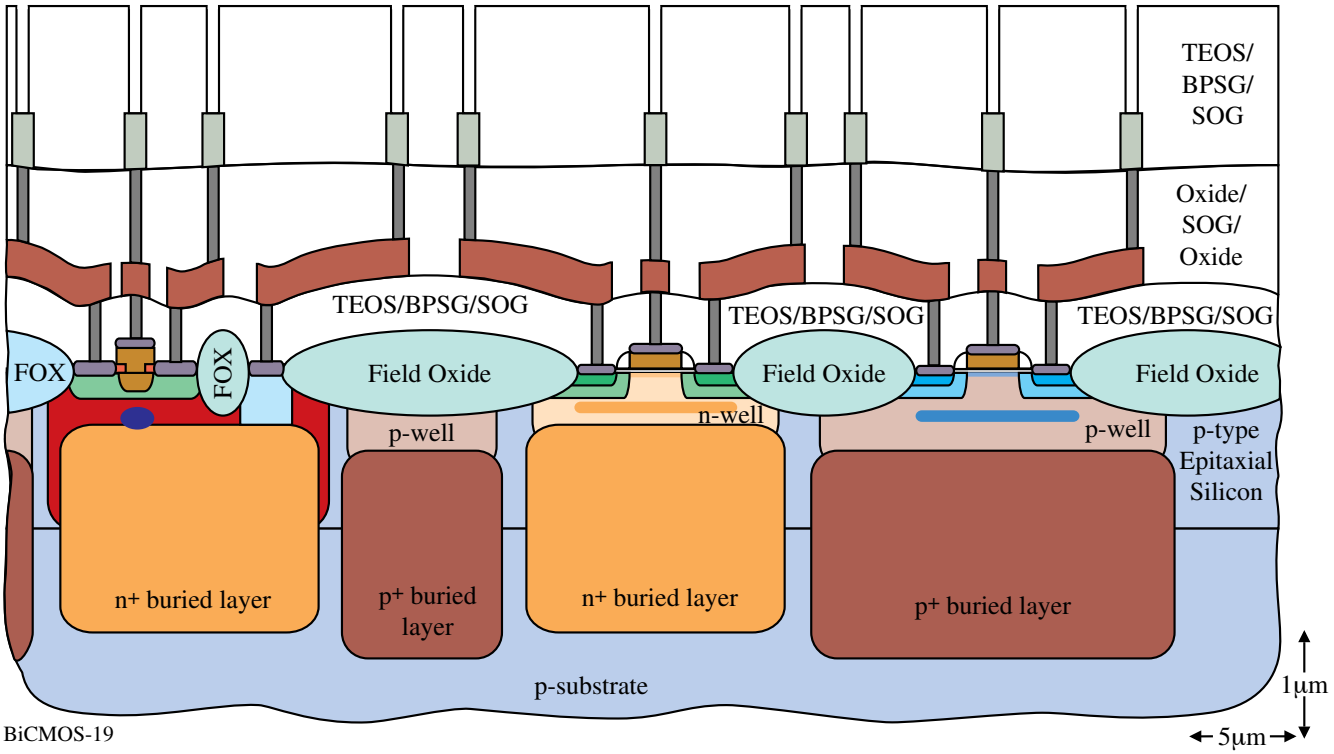
BiCMOS-17

Metal2



BiCMOS-18

Metal2-Metal3 Vias

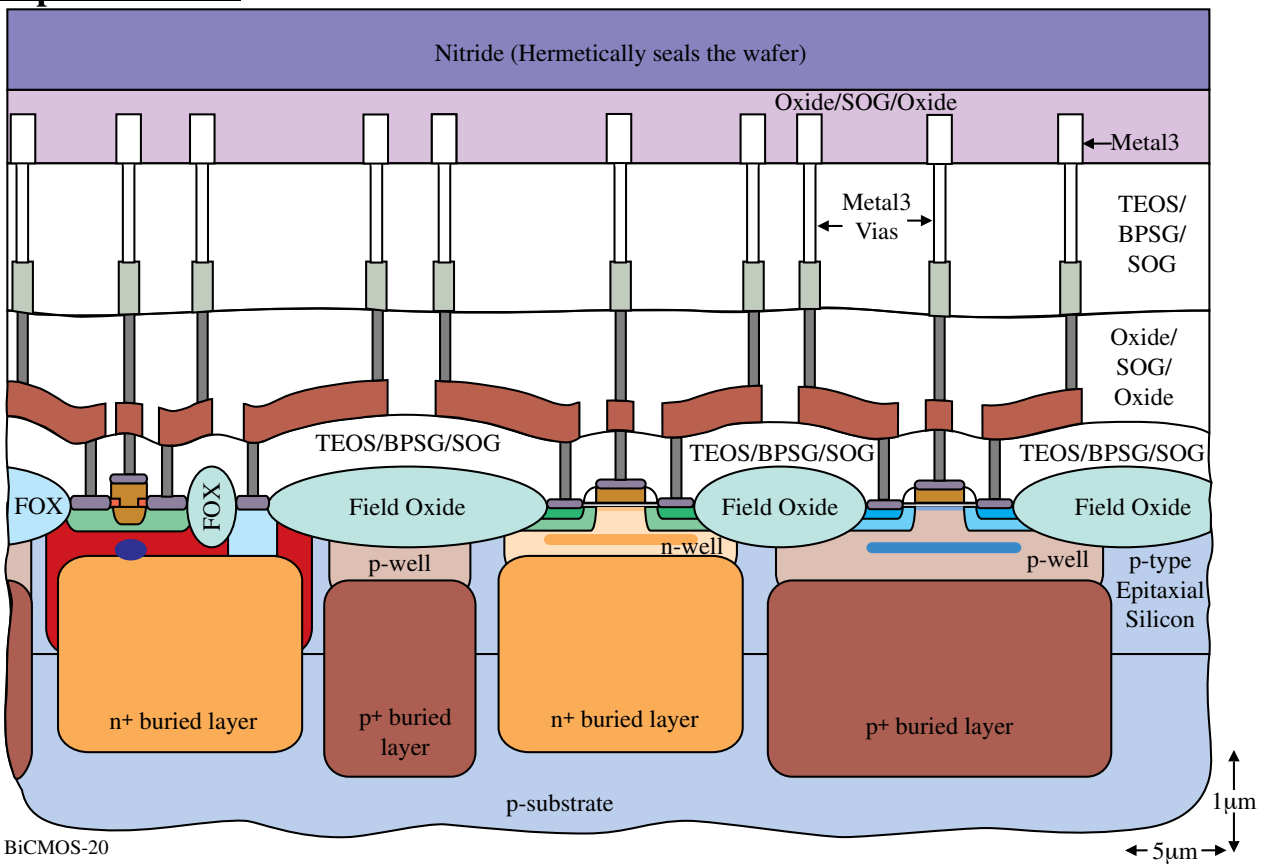


BiCMOS-19

Comments:

- The metal2-metal3 vias will be filled with metal3 as opposed to tungsten plugs

Completed Wafer



SUMMARY

- This section has illustrated the major process steps for a 0.5micron BiCMOS technology.
- The performance of the active devices are:

  npn bipolar junction transistor:

  f_T = 12GHz, β_F = 100-140 BV_{CEO} = 7V

  n-channel FET:

  K' = 127μA/V^2 V_T = 0.64V $\lambda_N \approx 0.060$

  p-channel FET:

  K' = 34μA/V^2 V_T = -0.63V $\lambda_P \approx 0.072$

- Although today's state of the art is 0.25μm to 0.13μm BiCMOS, the processing steps illustrated above approximate that which is done in a smaller geometry.