

REVIEW FOR EXAMINATION NO.2

Examination No. 2 will be given during class on Friday, March 5, 2004 from 12:05pm to 12:55pm. It will last for 50 minutes and is open book. The exam will consist of approximately 4 problems. Below is a list of the material for which you are responsible.

MOS Transistors

The summary in Sec. 2.9 is key to this section – you must know these formulas, what they mean and how to apply them for Exam 2.

MOS Inverter Circuits

Voltage transfer characteristic – V_{OH} , V_{OL} , V_{IH} , V_{IL} , V_S

Noise Margins (Multiple source noise margin)

Resistive load inverter design - V_{OH} , V_{OL} , V_{IH} , V_{IL} , V_S

NMOS transistor load inverters –

Saturated enhancement load – design of W/Ls

Linear enhancement load – design of W/Ls

CMOS inverters

- DC analysis

- Five regions of operation

- Finding V_{OH} , V_{OL} , V_{IH} , V_{IL} , V_S

Pseudo-NMOS inverters - V_{OH} , V_{OL} , V_{IH} , V_{IL} , V_S

Sizing of inverters – how to find the W/L ratios given the load capacitance

Understand how to use R_{eqn} and R_{eqp} and what they represent

Static MOS Gate Circuits

CMOS Gate Circuits – Inverter, NANDn and NORn (n = number of inputs)

Basic CMOS gate sizing

Implications of fanin and fanout

Voltage transfer characteristics for CMOS gates

Complex CMOS gates – be able to use the procedures outlined to synthesis a CMOS gate given the logic function

XOR and XNOR gates

Multiplexer circuits

Flip-Flops and latches

- Bistable

- SR latch with NOR gates and with NAND gates

JK Flip-Flop

- JK Master-slave flip-flop

- JK Edge-triggered flip-flop

D Flip-Flops and Latches

Power dissipation in CMOS gates

- Dynamic power (ignore glitch power)

- Static power (ignore leakage and subthreshold)

Power and delay tradeoffs