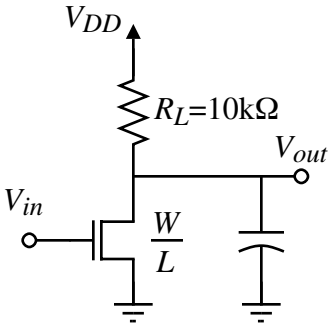
EXAMINATION NO. 2
(Average score = 70/100, Low 43, High 98)

Problem 1 - (25 points)

An NMOS transistor with a 10kΩ resistor as a load is used to implement a simple inverter as shown. The alpha-power model of Section 2.6 is used to fit the measured data for the NMOS transistor to produce the following two equations:

$$i_{DS} = (W/L)K_L(v_{GS} - V_{TN})v_{DS} \qquad v_{DS} \le V_{DS(\text{sat})}$$

$$i_{DS} = (W/L)K_S(v_{GS} - V_{TN})^{1.5} \qquad v_{DS} \ge V_{DS(\text{sat})}$$



where $K_L = 100\mu A/V^2$ and $K_S = 100\mu A/V^{1.5}$ and $V_{TN} = 0.6V$.

a.) Derive the expression for $V_{DS(\text{sat})}$ assuming the model above.

b.) Design V_{DD} and W/L of the resistively loaded inverter above to achieve $V_{OH} = 3.3V$ and $V_{OL} = 0.3V$.

c.) For the inverter of part b.) derive an expression for V_{IL} using the given alpha-power model. Using the previous values, evaluate V_{IL}.

Solution

a.) Equate the two equations for the linear and saturation regions to get,

$$\frac{W}{L}K_L(V_{GS}\text{-}V_{TN})V_{DS(\text{sat})} = \frac{W}{L}K_S(v_{GS} - V_{TN})^{1.5} \rightarrow \boxed{V_{DS(\text{sat})} = \frac{K_S}{K_L}\sqrt{v_{GS} - V_{TN}}}$$

b.) Since $V_{OH} = V_{DD}$, let $V_{DD} = \underline{\underline{3.3V}}$. Solve for V_{OL} by assuming the MOSFET is in the linear region.

$$\frac{V_{DD} - V_{OL}}{R_L} = \frac{3.3\text{-}0.3}{10k\Omega} = 300\mu A = \frac{W}{L}K_L(V_{DD} - V_{TN})V_{OL} = \frac{W}{L}\,100\mu A/V^2(3.3\text{-}0.6)0.3$$

$$\frac{W}{L} = \frac{300\mu A}{81\mu A} = \underline{\underline{3.7}}$$

c.) For V_{IL} assume the MOSFET is saturated. Therefore,

$$\frac{V_{DD} - V_{out}}{R_L} = \frac{W}{L}K_S(V_{in} - V_{TN})^{1.5}$$

Differentiating with respect to V_{in} gives,

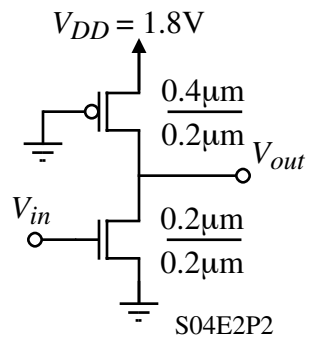
$$-\frac{1}{R_L}\frac{dV_{out}}{dV_{in}} = 1.5\,\frac{W}{L}K_S(V_{in} - V_{TN})^{0.5} \rightarrow \qquad \frac{1}{R_L} = 1.5\ (3.7)\ K_S(V_{IL} - V_{TN})^{0.5}$$

$$V_{IL} = V_{TN} + \frac{1}{[(1.5\cdot(W/L))K_S\,R_L]^2} = 0.6 + \frac{1}{(1.5\cdot 3.7\cdot 100\cdot 0.01)^2}$$

$$= 0.6 + 0.0325 = \underline{\underline{0.6325V}}$$

Problem 2 – (25 points)

For the pseudo-NMOS load inverter shown using 0.18μm CMOS technology, determine V_{OH} and estimateV_{OL} using the velocity saturated model with effective mobility (high vertical field). Be sure to clearly state any assumptions used in estimating V_{OL}.



Solution

For this inverter, we know that $V_{OH} \approx V_{DD} = \underline{\underline{1.8\text{V}}}$

For V_{OL}, we need to assume the state of the transistors. To help in this calculate $V_{DS(\text{sat})}$ for the NMOS and PMOS transistors.

$$\text{PMOS: } V_{SD(\text{sat})} = \frac{(V_{SG}-|V_{TP}|)E_{CP}L_P}{(V_{SG}-|V_{TP}|)+E_{CP}L_P} = \frac{(1.8\text{-}0.5)4.8}{(1.8\text{-}0.5)+4.8} = 1.023\text{V}$$

$$\text{NMOS: } V_{DS(\text{sat})} = \frac{(V_{GS}-V_{TN})E_{CN}L_N}{(V_{GS}-V_{TN})+E_{CN}L_N} = \frac{(1.8\text{-}0.5)1.2}{(1.8\text{-}0.5)+1.2} = 0.624\text{V}$$

So if $V_{OL} < 0.624$V, the PMOS is saturated and the NMOS is linear. Assuming this to be the case, we get:

$$\frac{W_n}{L_n}\frac{\mu_e C_{ox}}{1+\dfrac{V_{DS}}{E_{CN}L_N}}\left(V_{GS}-V_{TN}-\frac{V_{DS}}{2}\right)V_{DS} = W_p v_{sat} C_{ox}\frac{(V_{SG}-|V_{TP}|)^2}{(V_{SG}-|V_{TP}|)+E_{CP}L_P}$$

Assuming V_{DS} which is V_{OL} is small, we can simplify the above to,

$$\frac{W_n}{L_n}\mu_e(V_{GS}-V_{TN})V_{OL} \approx W_p v_{sat}\frac{(V_{SG}-|V_{TP}|)^2}{(V_{SG}-|V_{TP}|)+E_{CP}L_P}$$

Substituting the values gives,

$$270(\text{cm}^2/\text{v}\cdot\text{s})(1.8\text{-}0.5)V_{OL} = 0.4\text{x}10^{-4}(\text{cm})(8\text{x}10^6)(\text{cm/s})\frac{(1.8\text{-}0.5)^2}{1.8\text{-}0.5+4.8}$$

$$351V_{OL} = 88.656 \quad \rightarrow \quad V_{OL} = \underline{\underline{0.253\text{V}}}$$

This problem can also be solved exactly for V_{OL} as follows.

$$\frac{270(1.8\text{-}0.5\text{-}0.5V_{OL})V_{OL}}{1+V_{OL}/1.2} = (0.4\text{x}10^{-4})(8\text{x}10^6)\frac{(1.8\text{-}0.5)^2}{1.8\text{-}0.5+4.8} = 88.656$$

$$270(1.3\text{-}0.5V_{OL})V_{OL} = 88.656(1+0.833V_{OL})$$

$$351V_{OL} - 135V_{OL}^2 = 88.656 + 73.88V_{OL}$$

$$\therefore \quad 135V_{OL}^2 + (73.88\text{-}351)V_{OL} + 88.656 = 0 \rightarrow V_{OL}^2 - 2.053V_{OL} + 0.6567 = 0$$

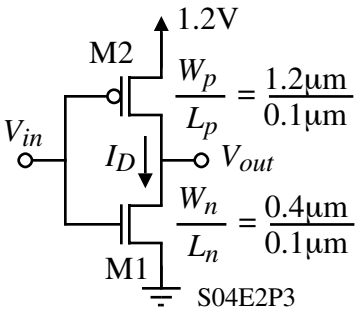
$$V_{OL} = 1.0265 \pm 0.5\sqrt{2.053^2\text{-}4\cdot 0.6567} = 1.0265 \pm 0.5\sqrt{1.588} = 1.0265 \pm 0.6300$$

$$\therefore \quad V_{OL} = \underline{\underline{0.3964\text{V}}}$$

Either answer will be accepted provided the work is correct and the assumptions consistent.

Problem 3 – (25 points)

The CMOS inverter shown uses 0.13μm CMOS technology. a.) Sketch the voltage transfer characteristic of the standard CMOS inverter shown. Label the points on this curve that separate the various regions of operation for the MOSFETs. Estimate the location of these points as close as possible without numerical calculations. b.) How far can the power supply, V_{DD}, be reduced before the inverter fails to operate correctly? c.) Sketch a graph of the dc current transfer characteristic versus the input voltage for the above inverter. Compute the peak value of current and label all important points along the characteristic.



Solution

a.) Assuming that $V_S \approx 0.6$V, the sketch of the voltage transfer characteristic is shown. (Actually, V_S can be calculated as 0.586V where $\chi = 1.155$)

PMOS:

$$V_{SD(sat)} = \frac{(V_{SG} - |V_{TP}|)E_{CP}L_P}{(V_{SG} - |V_{TP}|) + E_{CP}L_P}$$

$$V_{SD(sat)} \approx V_{SG} - |V_{TP}|$$

if $V_{SG} - |V_{TP}| < E_{CP}L_P$

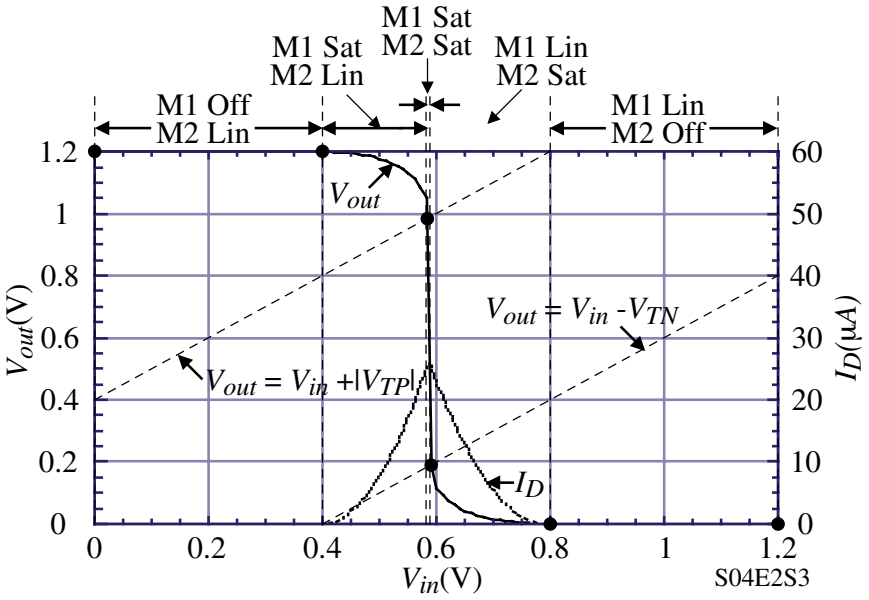
This can be rewritten as,

$V_{out} = V_{in} + |V_{TP}|$ and is plotted on the curve.

NMOS:

A similar analysis gives,

$V_{out} = V_{in} - V_{TN}$ and is plotted on the curve.



b.) The lowest power supply voltage is $V_{TN} = |V_{TP}| = \underline{0.4\text{V}}$. Otherwise, one of the transistors would not turn on and the output could not be pulled to V_{DD} or ground. This answer ignores subthreshold.

c.) The sketch of the dc transfer current is shown on the sketch. It only flows when neither transistor is off. The peak value can be calculated assuming the transistors are in saturation.

$$I_{DS}(\text{peak}) = W_p v_{sat} C_{ox} \frac{(V_{GS} - V_{TN})^2}{(V_{GS} - V_{TN}) + E_{CN}L_N} = \frac{(0.4\text{x}10^{-4})(8\text{x}10^{6})(1.5\text{x}10^{-6})(0.2)^2}{0.2+0.6}$$

$$I_{DS}(\text{peak}) = \underline{\underline{25.6\mu\text{A}}}$$

(This assumes that $V_{GS} = 0.6$V. If we use $V_{GS} = 0.586$V the current is 22.45μA))

Problem 4 – (25 points)

Using a complex CMOS logic, implement the function, F = AB +C. Assume that each input and its complement are available. Assuming all transistors have the same length, size the widths to implement the FO4 rules (the worst case pull-up and pull-down is identical to an inverter with $W_p = 2W$ and $W_n = W$). What is the value of W for this logic gate if $t_{PLH} = t_{PHL} = 50\text{ps}$, $L = 0.1\mu\text{m}$, and $C_L = 100\text{fF}$?

Solution

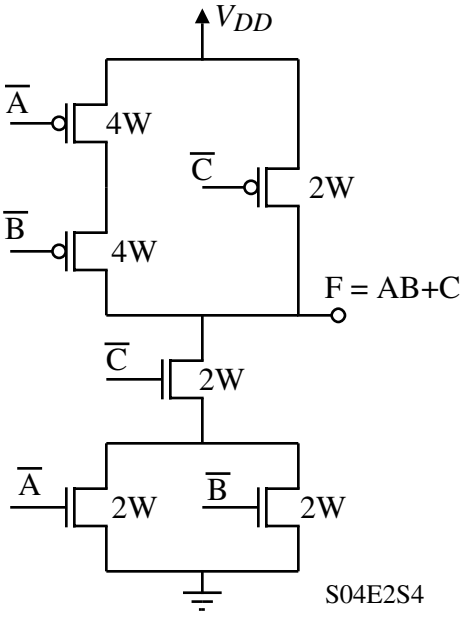
NMOS complex:

$$\overline{F} = \overline{AB+C} = (\overline{A} + \overline{B})\,\overline{C}$$

PMOS complex:

$$F = \overline{A}\,\overline{B} + \overline{C} \text{ which is the dual of } \overline{F}$$

Therefore, the CMOS logic implementation is shown along with the sizing that satisfies the FO4 rules.



The value of W can be found as follows,

$$t_{PHL} = t_{PLH} = 50\text{ps} = 0.7R_{eff}C_L$$

$$50\text{ps} = 0.7R_{eqn}(L/W)C_L$$

$$= 0.7(12.5\text{k}\Omega)(L/W)100\text{fF}$$

$$\therefore\ W/L = \frac{0.7\cdot 12.5\text{x}10^3\cdot 100\text{fF}}{50\text{ps}} = 17.5$$

$$W = 17.5(0.1\mu\text{m}) = \underline{\underline{1.75\mu\text{m}}}$$