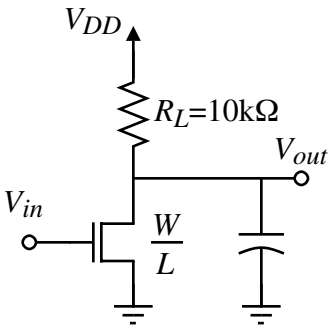
EXAMINATION NO. 2

NAME_____SCORE_____/100

INSTRUCTIONS: This exam is open textbook only. The exam consists of 4 questions for a total of 100 points. Please show your work leading to your answers so that maximum partial credit may be given where appropriate. Be sure to turn in your exam with the problems in numerical order, firmly attached together.

Problem 1 - (25 points)

An NMOS transistor with a 10kΩ resistor as a load is used to implement a simple inverter as shown. The alpha-power model of Section 2.6 is used to fit the measured data for the NMOS transistor to produce the following two equations:



$$i_{DS} = (W/L)K_L(v_{GS} - V_{TN})v_{DS} \qquad v_{DS} \le V_{DS(\text{sat})}$$

$$i_{DS} = (W/L)K_S(v_{GS} - V_{TN})^{1.5} \qquad v_{DS} \ge V_{DS(\text{sat})}$$

where $K_L = 100\mu A/V^2$ and $K_S = 100\mu A/V^{1.5}$ and $V_{TN} = 0.6V$.

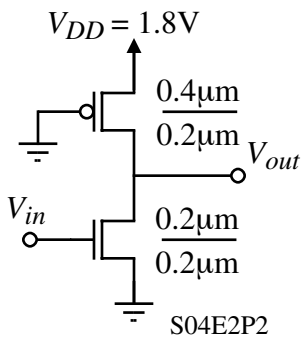
a.) Derive the expression for $V_{DS(\text{sat})}$ assuming the model above.

b.) Design V_{DD} and W/L of the resistively loaded inverter above to achieve $V_{OH} = 3.3V$ and $V_{OL} = 0.3V$.

c.) For the inverter of part b.) derive an expression for V_{IL} using the given alpha-power model. Using the previous values, evaluate V_{IL}.

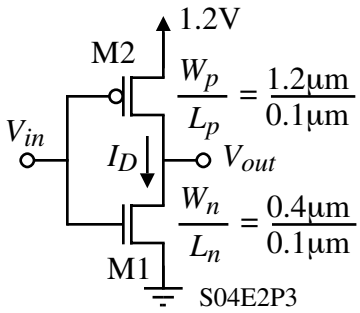
Problem 2 – (25 points)

For the pseudo-NMOS load inverter shown using 0.18μm CMOS technology, determine V_{OH} and estimate V_{OL} using the velocity saturated model with effective mobility (high vertical field). Be sure to clearly state any assumptions used in estimating V_{OL}.



Problem 3 – (25 points)

The CMOS inverter shown uses 0.13μm CMOS technology. a.) Sketch the voltage transfer characteristic of the standard CMOS inverter shown. Label the points on this curve that separate the various regions of operation for the MOSFETs. Estimate the location of these points as close as possible without numerical calculations. b.) How far can the power supply, V_{DD}, be reduced before the inverter fails to operate correctly? c.) Sketch a graph of the dc current transfer characteristic versus the input voltage for the above inverter. Compute the peak value of current and label all important points along the characteristic.



Problem 4 – (25 points)

Using a complex CMOS logic, implement the function, F = AB +C. Assume that each input and its complement are available. Assuming all transistors have the same length, size the widths to implement the FO4 rules (the worst case pull-up and pull-down is identical to an inverter with $W_p = 2W$ and $W_n = W$). What is the value of W for this logic gate if $t_{PLH} = t_{PHL}$ = 50ps, L = 0.1μm, and C_L = 100fF?

Extra Sheet