REVIEW FOR EXAMINATION NO.3

Examination No. 3 will be given during class on Wednesday, April 14, 2004 from 12:05pm to 12:55pm. It will last for 50 minutes and is open book. The exam will consist of approximately 4 problems. Below is a list of the material for which you are responsible.

**MOS Transistors**

The summary in Sec. 2.9 is key to this section – you must know these formulas, what they mean and how to apply them for Exam 3.

**High-Speed CMOS Logic Design**

Switching time analysis – Inverter and gate delay calculations
Gate capacitance – how to calculate and use
Self capacitance – how to calculate and use
Wire capacitance – how to use
Gate sizing for optimal path delay
   - Relationships that give optimal delay
     - Figure 6.23 – meaning and application
Optimizing paths with inverters, NANDs or NORs
Optimizing paths using logic effort for general path delay optimization
Branching and sideloads

**Transfer Gate and Dynamic Logic Design**

CMOS Gate Circuits – Inverter, NANDn and NORn (n = number of inputs)
   - Characteristics and limitations
   - Clock feedthrough
   - Capacitive sharing
CMOS transmission gate logic, multiplexers
Delay of CMOS transmission gates
Logical effort with CMOS transmission gates
Dynamic D-latches and D Flip-flops
Domino (Dynamic) Logic
Design of domino logic functions
Limitations of domino logic
Differential domino logic
Power and delay tradeoffs

**Semiconductor Memory Design**

Memory organization
Types of memories
MOS decoders – single and multiple-level
SRAM cell design
   - Function of the transistors
   - Read operation
   - Write operation
SRAM column I/O circuitry
   - Pull-ups
   - Column selection
   - Write circuits
Read circuits – sense amplifiers, latches, combination of amplifier and latches