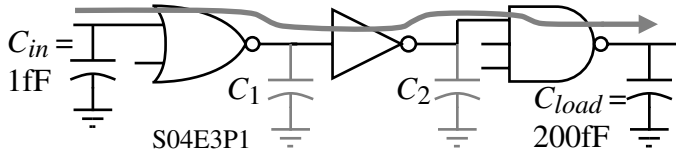
EXAMINATION NO. 3 - SOLUTIONS

(Average score = 65/100)

Problem 1 - (30 points)

Find the optimum delay and the device sizes in each of the logic circuits below for the path shown using optimal path delay concepts. Assume that the channel length of all transistors is 0.1μm and that the technology corresponds to 0.13μm CMOS technology.



Solution

$$\text{Fanout Delay} = \left[\tau_{\text{nor2}}\left(\frac{C_1}{C_{in}}\right)\tau_{\text{inv}}\left(\frac{C_2}{C_1}\right)\tau_{\text{nand3}}\left(\frac{C_{\text{load}}}{C_2}\right)\right]^{1/3} = \left[\tau_{\text{nor2}}\tau_{\text{inv}}\tau_{\text{nand3}}\left(\frac{C_{\text{load}}}{C_{in}}\right)\right]^{1/3}$$

$\tau_{\text{nor2}} = \tau_{\text{nand3}} = 5R_{eqn}C_gL_n = 5\cdot 12.5\text{k}\cdot 2\text{fF/μm}\cdot 0.1\text{μm} = 12.5\text{ps}$

$\tau_{inv} = 3R_{eqn}C_gL_n = 3\cdot 12.5\text{k}\cdot 2\text{fF/μm}\cdot 0.1\text{μm} = 7.5\text{ps}$

$\therefore$ Fanout Delay $= [5\cdot 3\cdot 5\cdot (C_{load}/C_{in})]^{1/3}R_{eqn}C_gL_n = (5\cdot 3\cdot 5\cdot 200)^{1/3}R_{eqn}C_gL_n$

$= (5\cdot 3\cdot 5\cdot 200)^{1/3}R_{eqn}C_gL_n = 15{,}000^{1/3}R_{eqn}C_gL_n = 24.662\ R_{eqn}C_gL_n$

Setting each stage fanout-delay equal to this term gives the input capacitances working from the output back to the input.

$$C_2 = \frac{5C_{load}}{24.662} = \frac{5\cdot 200\text{fF}}{24.662} = 40.55\text{fF}, \qquad C_1 = \frac{3C_2}{24.662} = \frac{5\cdot 40.55\text{fF}}{24.662} = 4.932\text{fF}$$

Checking C_{in} gives, $C_{in} = \dfrac{5C_1}{24.662} = \dfrac{5\cdot 4.932\text{fF}}{24.662} = 1\text{fF}$

Next, set each gate delay equal to $R_{eff}C_{in} = R_{eqn}\left(\dfrac{L_n}{W}\right)C_{in}$ to find W.

NOR2: $5R_{eqn}C_gL_n = R_{eqn}\left(\dfrac{L_n}{W}\right)C_{in} \rightarrow W = \dfrac{C_{in}}{5C_g} = \dfrac{1\text{fF}}{5\cdot 2\text{fF/μm}} = 0.1\text{μm}$

$\therefore$ $W_n = W = \underline{\underline{0.1\text{μm}}}$ and $W_p = 4W = \underline{\underline{0.4\text{μm}}}$

INV: $3R_{eqn}C_gL_n = R_{eqn}\left(\dfrac{L_n}{W}\right)C_1 \rightarrow W = \dfrac{C_1}{3C_g} = \dfrac{4.932\text{fF}}{3\cdot 2\text{fF/μm}} = 0.82\text{μm}$

$\therefore$ $W_n = W = \underline{\underline{0.82\text{μm}}}$ and $W_p = 2W = \underline{\underline{0.164\text{μm}}}$

NAND3: $5R_{eqn}C_gL_n = R_{eqn}\left(\dfrac{L_n}{W}\right)C_2 \rightarrow W = \dfrac{C_2}{5C_g} = \dfrac{40.55\text{fF}}{5\cdot 2\text{fF/μm}} = 4.055$

$\therefore$ $W_n = 3W = \underline{\underline{12.16\text{μm}}}$ and $W_p = 2W = \underline{\underline{8.11\text{μm}}}$

$$\text{Total delay} = \tau_{\text{nand3}}\left(\frac{200}{40.55}+\gamma_{\text{nand3}}\right) + \tau_{\text{inv}}\left(\frac{40.55}{4.932}+\gamma_{\text{inv}}\right) + \tau_{\text{nor2}}\left(\frac{4.932}{1}+\gamma_{\text{nor2}}\right)$$

$\gamma_{\text{nand3}} = \dfrac{C_{self}}{C_{in}} = \dfrac{13WC_{eff}}{5WC_g} = \dfrac{13\cdot 1}{5\cdot 2} = 1.3$, $\gamma_{\text{inv}} = 0.5$, $\gamma_{\text{nor2}} = \dfrac{(W_n+W_p+W_p)C_{eff}}{4WC_g} = \dfrac{6\cdot 1}{4\cdot 2} = 0.75$

$\therefore$ Total delay = 12.5ps(4.932+1.3) + 7.5ps(8.22+0.5) + 12.5ps(4.932+0.75) = $\underline{\underline{214\text{ps}}}$

Problem 2 – (25 points)

For the logic circuit in Problem 1, find the optimum delay and the device sizes in each of the logic circuits below for the path shown using logical effort concepts. Assume that the channel length of all transistors is 0.1μm and that the technology corresponds to 0.13μm CMOS technology.

Solution

Total path effort = $PE = LE_{\text{nor2}}\text{x}LE_{\text{inv}}\text{x}LE_{\text{nand3}}\text{x}\dfrac{C_{load}}{C_{in}} = \left(\dfrac{5}{3}\right)(1)\left(\dfrac{5}{3}\right)\left(\dfrac{200}{1}\right) = 555.55$

Stage effort = $SE = (555.55)^{1/3} = 8.22$

Delay = $D = 3(8.22) + 1.5 + 0.5 + 1.5 = 28.162$

Minimum path delay = $D\ \text{x}\tau_{\text{inv}}$ 28.162x7.5ps = 211.2ps

Working backwards from the output to the input we compute the input capacitances:

$$LE_{\text{nand3}}\left(\frac{C_{load}}{C_2}\right) = 8.22 \quad \rightarrow \quad C_2 = \frac{LE_{\text{nand3}}C_{load}}{8.22} = \frac{(5/3)\text{x}100\text{fF}}{8.22} = 40.55\text{fF}$$

$$LE_{\text{inv}}\left(\frac{C_2}{C_1}\right) = 8.22 \quad \rightarrow \quad C_1 = \frac{LE_{\text{inv}}C_2}{8.22} = \frac{(1)\text{x}40.55\text{fF}}{8.22} = 4.932\text{fF}$$

$$Le_{\text{nor2}}\left(\frac{C_{load}}{C_2}\right) = 8.22 \quad \rightarrow \quad C_2 = \frac{LE_{\text{nor2}}C_1}{8.22} = \frac{(5/3)\text{x}4.932\text{fF}}{8.22} = 1\text{fF}$$

Next, set each gate delay equal to $R_{eff}C_{in} = R_{eqn}\left(\dfrac{L_n}{W}\right)C_{in}$ to find W.

NOR2: $5R_{eqn}C_gL_n = R_{eqn}\left(\dfrac{L_n}{W}\right)C_{in} \rightarrow W = \dfrac{C_{in}}{5C_g} = \dfrac{1\text{fF}}{5\cdot 2\text{fF/μm}} = 0.1\text{μm}$

$\therefore \quad W_n = W = 0.1\text{μm}$ and $W_p = 4W = 0.4\text{μm}$

INV: $3R_{eqn}C_gL_n = R_{eqn}\left(\dfrac{L_n}{W}\right)C_1 \rightarrow W = \dfrac{C_1}{3C_g} = \dfrac{4.932\text{fF}}{3\cdot 2\text{fF/μm}} = 0.82\text{μm}$

$\therefore \quad W_n = W = 0.82\text{μm}$ and $W_p = 2W = 0.164\text{μm}$

NAND3: $5R_{eqn}C_gL_n = R_{eqn}\left(\dfrac{L_n}{W}\right)C_2 \rightarrow W = \dfrac{C_2}{5C_g} = \dfrac{40.55\text{fF}}{5\cdot 2\text{fF/μm}} = 4.055$

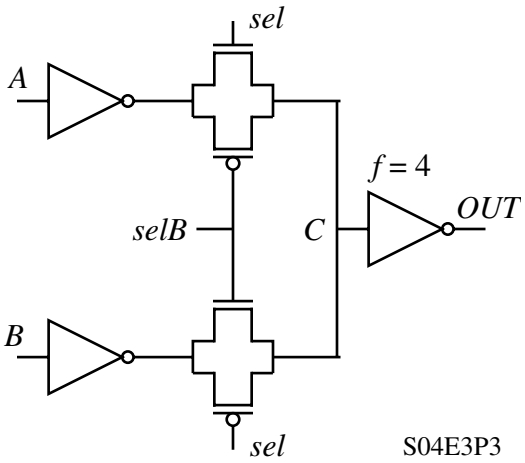
$\therefore \quad W_n = 3W = 12.16\text{μm}$ and $W_p = 2W = 8.11\text{μm}$

Total delay $= \tau_{\text{nand3}}\left(\dfrac{200}{40.55}+\gamma_{\text{nand3}}\right) + \tau_{\text{inv}}\left(\dfrac{40.55}{4.932}+\gamma_{\text{inv}}\right) + \tau_{\text{nor2}}\left(\dfrac{4.932}{1}+\gamma_{\text{nor2}}\right)$

$\gamma_{\text{nand3}} = \dfrac{C_{self}}{C_{in}} = \dfrac{13WC_{eff}}{5WC_g} = \dfrac{13\cdot 1}{5\cdot 2} = 1.3$, $\gamma_{\text{inv}} = 0.5$, $\gamma_{\text{nor2}} = \dfrac{(W_n+W_p+W_p)C_{eff}}{4WC_g} = \dfrac{6\cdot 1}{4\cdot 2} = 0.75$

Problem 3 – (25 points)

For the logic circuit shown below, assume that the transmission gates are all 4λ:2λ and that the inverters driving the transmission gates have PMOS transistors that are 8λ:2λ, and NMOS transistors that are 4λ:2λ, where λ = 0.1μm. The output inverter is to drive a 50 fF load. The output inverter is 4 times larger than the input inverters.



S04E3P3

(a.) Write the logic expression for the output function in terms of *A*, *B*, *sel*, and *selB*.

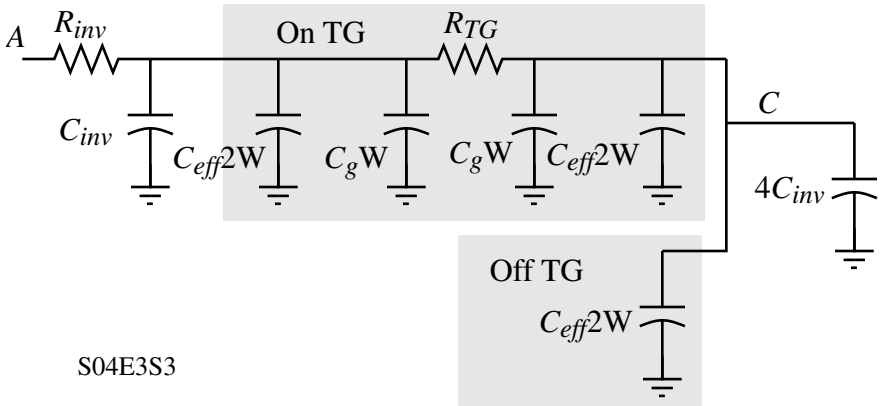
(b.) Draw an equivalent *RC* circuit model for the path from *A* to *C* assuming that the *sel* signal is high. Write down the individual contributions for each resistance and capacitance and place the total values at the appropriate nodes.

(c.) Find the Elmore delay from *A* to *C*.

Solution

(a.) $OUT = \overline{sel\cdot\overline{A} + \overline{sel}\cdot\overline{A}} = (\overline{sel} + A)\cdot(sel\cdot B) = A\cdot sel + B\cdot selB$

(b.) The equivalent *RC* circuit model is shown below.



S04E3S3

The quantities in this model are:

$R_{inv} = 12.5k\Omega\left(\frac{2\lambda}{4\lambda}\right) = 6.25k\Omega$, $C_{inv} = C_{eff}(W_n+W_p) = 1fF/\mu m(0.4\mu m+0.8\mu m) = 1.2fF$,

$C_{eff}(2W) = 1fF/\mu m(0.8\mu m) = 0.8fF$, $C_gW = 2fF/\mu m(0.4\mu m) = 0.8fF$

$R_{TG} = 12.5k\Omega\left(\frac{2\lambda}{4\lambda}\right) = 6.25k\Omega$, and $4C_{inv} = 4C_gW = 4(2fF/\mu m)(1.2\mu m) = 9.6fF$

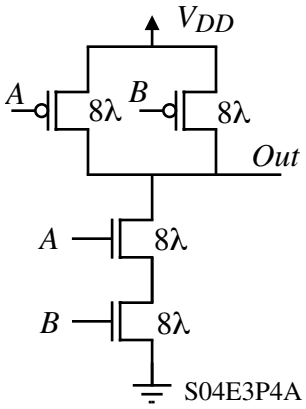
(c.) The Elmore delay from *A* to *C* is given as

$t_{AC} = 6.25k\Omega(1.2fF+0.8fF+0.8fF) + (6.25k\Omega+6.25k\Omega)(0.8fF+0.8fF+0.8fF+9.6fF)$

$= 6.25k\Omega(2.8fF) + 6.25k\Omega(12fF) = 17.5ps + 150ps = \underline{\underline{167.5ps}}$

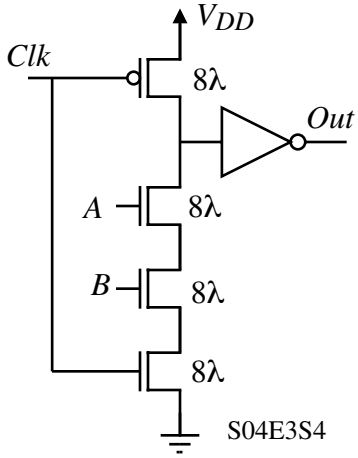
Problem 4 – (20 points)

(a.) Find the equivalent dynamic gate of the static logic gate shown. (b.) Find the logical effort for both gates.



Solution

(a.) The equivalent circuit is shown where the clock is assumed to arrive first before *A* and *B*.



(b.) Both gates have equal rise and fall times. Therefore the logical effort for both gates is as follows:

$$LE_{static} = \frac{8\lambda+8\lambda}{4\lambda+8\lambda} = \frac{16}{12} = \frac{4}{3} = \underline{\underline{1.33}}$$

$$LE_{dynamic} = \frac{8\lambda}{4\lambda+8\lambda} = \frac{8}{12} = 2/3 = \underline{\underline{0.67}}$$