# EXAMINATION  NO.  3

NAME_____SCORE_____/100

INSTRUCTIONS:  This exam is open textbook only.  The exam consists of 4 questions for a total of 100 points.  Please show your work leading to your answers so that maximum partial credit may be given where appropriate.  Be sure to turn in your exam with the problems in numerical order, firmly attached together.

## Problem  1 - (30  points)

Find the optimum delay and the device sizes in each of the logic circuits below for the path shown using optimal path delay concepts.  Assume that the channel length of all transistors is 0.1µm and that the technology corresponds to 0.13µm CMOS technology.



$C_{in} = 1fF$    $C_1$    $C_2$    $C_{load} = 200fF$

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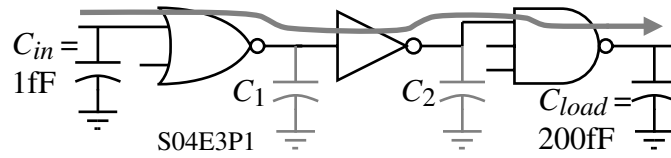
## Problem 2 – (25 points)

For the logic circuit in Problem 1, find the optimum delay and the device sizes in each of the logic circuits below for the path shown using logical effort concepts. Assume that the channel length of all transistors is 0.1μm and that the technology corresponds to 0.13μm CMOS technology.

## Problem 3 – (20 points)

For the logic circuit shown below, assume that the transmission gates are all 4λ:2λ and that the inverters driving the transmission gates have PMOS transistors that are 8λ:2λ, and NMOS transistors that are 4λ:2λ, where λ = 0.1μm. The output inverter is to drive a 50 fF load. The output inverter is 4 times larger than the input inverters.
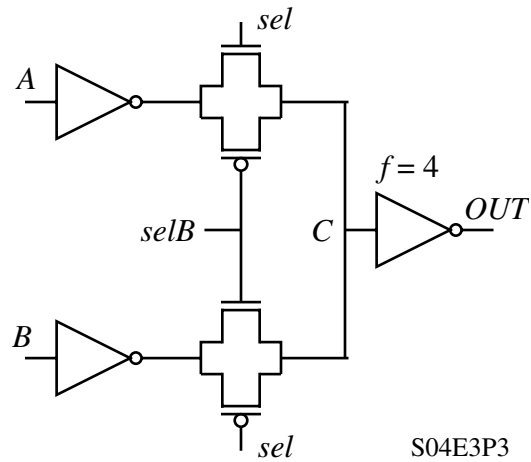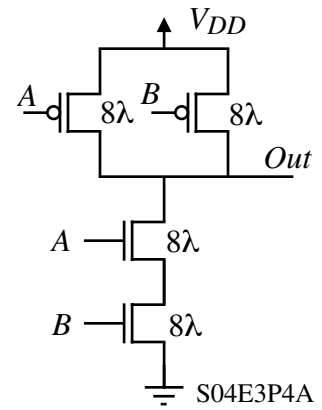
(a.) Write the logic expression for the output function in terms of $A$, $B$, $sel$, and $selB$.

(b.) Draw an equivalent $RC$ circuit model for the path from $A$ to $C$ assuming that the $sel$ signal is high. Write down the individual contributions for each resistance and capacitance and place the total values at the appropriate nodes.

(c.) Find the Elmore delay from $A$ to $C$.

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## Problem 4 – (25 points)

(a.) Find the equivalent dynamic gate of the static logic gate shown. (b.) Find the logical effort for both gates.

$V_{DD}$

$A$ ―◁| 8λ   $B$ ―◁| 8λ

$Out$

$A$ ―| 8λ

$B$ ―| 8λ

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Extra Sheet