REVIEW FOR FINAL EXAMINATION

The Final Examination will be given Tuesday, April 27, 2004 from 8:00am to 10:50am. The exam is open book. The exam is open book and will consist of approximately 7 problems of which 5 problems, each worth 20 points for a total of 100 points, must be worked. The 7 problems will fall into two categories, those you must work and those you may work. Below is a list of the material for which you are responsible.

Deep Submicron Digital IC Design

Review of Digital Logic Gate Design
Basic logic functions
    - DeMorgan's Laws
    - Sequential Logic Circuits
Implementation of Logic Circuits
    - Characteristics
Noise Margins
Propagation Delay Time
Power
    - Static
    - Dynamic

MOS Transistors

Structure and operation of MOSFETs
    - Equivalent ON and OFF resistances
Threshold voltage of the MOSFET
    - Equation (2.11) – its components and their meaning and the parameters of Eq. (2.11)
Development and application of the First-Order (Sah model) Current-Voltage
    Characteristics
Development and application of the Velocity-Saturated Current-Voltage Model
Application and understanding of the Subthreshold Conduction Model
Capactances of the MOSFET
    - Thin-oxide (intrinsic capacitances)
    - PN-junction capacitances (depletion capacitances)
    - Overlap capacitances (intrinsic capacitances)
The summary in Sec. 2.9 is key to this section – you must know these formulas, what they
    mean and how to apply them.

Fabrication, Layout and Simulation

IC Fabrication Technology
    - What are the five major processing steps in IC technology? Also you should know
      about the epitaxial process
    - Photolithography process – what is it and how is it applied
    - Know the physical aspects of the MOSFET – cross-section
    - Connections – metal, vias, etc.
Calculation of capacitance and resistance of a conductor
Calculating the resistance and capacitance associated with the physical layout of a MOSFET
Circuit simulation models for the MOSFET
    SPICE – Level 1 model and parameters
Extraction of the level 1 model parameters
Temperature dependence of MOSFETs for the various regions of operation
Voltage limitations
Latchup

MOS Inverter Circuits

Voltage transfer characteristic – V_{OH}, V_{OL}, V_{IH}, V_{IL}, V_S
Noise Margins (Multiple source noise margin)
Resistive load inverter design - V_{OH}, V_{OL}, V_{IH}, V_{IL}, V_S
NMOS transistor load inverters –
    Saturated enhancement load – design of W/Ls
    Linear enhancement load – design of W/Ls
CMOS inverters
    - DC analysis
    - Five regions of operation
    - Finding V_{OH}, V_{OL}, V_{IH}, V_{IL}, V_S
Pseudo-NMOS inverters - V_{OH}, V_{OL}, V_{IH}, V_{IL}, V_S
Sizing of inverters – how to find the W/L ratios given the load capacitance
Understand how to use R_{eqn} and R_{eqp} and what they represent

Static MOS Gate Circuits

CMOS Gate Circuits – Inverter, NANDn and NORn (n = number of inputs)
Basic CMOS gate sizing
Implications of fanin and fanout
Voltage transfer characteristics for CMOS gates
Complex CMOS gates – be able to use the procedures outlined to synthesis a CMOS gate
    given the logic function
XOR and XNOR gates
Multiplexer circuits
Flip-Flops and latches
    - Bistable
    - SR latch with NOR gates and with NAND gates
JK Flip-Flop
    - JK Master-slave flip-flop
    - JK Edge-triggered flip-flop
D Flip-Flops and Latches
Power dissipation in CMOS gates
    - Dynamic power (ignore glitch power)
    - Static power (ignore leakage and subthreshold)
Power and delay tradeoffs

High-Speed CMOS Logic Design

Switching time analysis – Inverter and gate delay calculations
Gate capacitance – how to calculate and use
Self capacitance – how to calculate and use
Wire capacitance – how to use
Gate sizing for optimal path delay
       Relationships that give optimal delay
       Figure 6.23 – meaning and application
Optimizing paths with inverters, NANDs or NORs
Optimizing paths using logic effort for general path delay optimization
Branching and sideloads

Transfer Gate and Dynamic Logic Design

CMOS Gate Circuits – Inverter, NANDn and NORn (n = number of inputs)
    Characteristics and limitations
    Clock feedthrough
    Capacitive sharing

CMOS transmission gate logic, multiplexers
Delay of CMOS transmission gates
Logical effort with CMOS transmission gates
Dynamic D-latches and D Flip-flops
Domino (Dynamic) Logic
Design of domino logic functions
Limitations of domino logic
Differential domino logic
Power and delay tradeoffs

Semiconductor Memory Design

Memory organization
Types of memories
MOS decorders – single and multiple-level
SRAM cell design
 Function of the transistors
 Read operation
 Write operation
SRAM column I/O circuitry
 Pull-ups
 Column selection
 Write circuits
  Read circuits – sense amplifiers, latches, combination of amplifier and latches

Interconnect Design

Interconnect RC delays
 Wire resistance, wire capacitance
Elmore delay
RC delay in long wires
Buffer insertion to reduce delay in long wires
Interconnect coupling capacitance
 Components
 Models
 Agressor-victim coupling
Interconnect inductance
Antenna effects

Power Grid and Clock Design

Power distribution
 IR drop and Ldi/dt drop
Power routing
Clock and timing issues
 Clock skew, influence of noise on the clocks
Power dissipation in clocks
Clock generation and distribution
Phase-locked loops/delay locked loops
PLL design