

FINAL EXAMINATION - SOLUTIONS

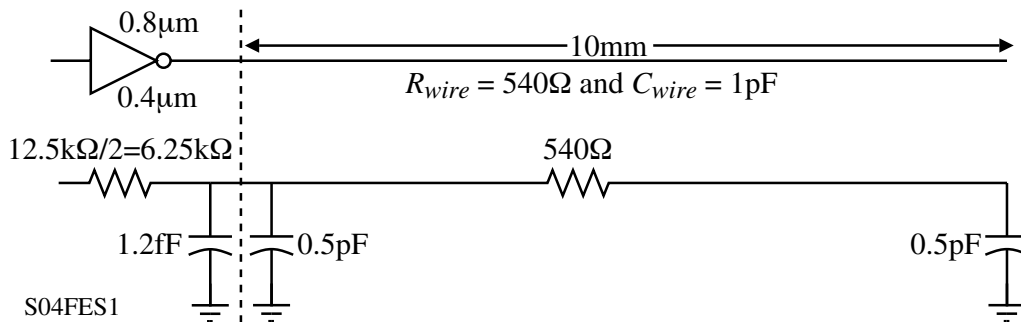
(Average score = 68/100)

Problem 1 - (20 points – This problem is required)

- a.) An interconnect line is 10 mm long and has a resistance of $54\text{m}\Omega/\mu\text{m}$ and a capacitance of $0.1\text{fF}/\mu\text{m}$ and is driven by a 2X inverter (an inverter with an 8λ PMOS and a 4λ NMOS where $\lambda = 0.1\mu\text{m}$). What is the total delay of the circuit from the input of the inverter to the end of the interconnect line?
- b.) Find the number of buffers (round off to the nearest integer) and the size of these buffers to minimize the delay of the 10 mm interconnect through buffer insertion.
- c.) Since the X2 buffer probably cannot drive the insertion buffer at the input directly, use a fanout of 4 (FO4) to design a cascade of inverters that will allow the X2 buffer at the input to drive the first insertion buffer with minimum delay.
- d.) For your design above which includes the cascade of inverters at the input followed by the buffer insertion in the 10 mm interconnect, compute the delay value from the 2X inverter at the input to the end of the interconnect. Assume that the average FO4 delay of the cascaded inverters is 100ps.

Solution

a.)



$$\tau \approx (6.25\text{k}\Omega)(0.5\text{pF}) + (6.79\text{k}\Omega)(0.5\text{pF}) = \underline{6.52\text{ns}}$$

b.) Find the number of inserted buffers, N , and the size of each buffer, M .

$$N = \sqrt{\frac{R_{\text{wire}} C_{\text{wire}} / 2}{R_{\text{eqn}} (C_J + C_G) (1 + \beta)}} = \sqrt{\frac{0.5 \cdot 540 \cdot 1\text{pF}}{12.5\text{k}\Omega (1\text{fF} \cdot 0.2 \cdot 3 + 2\text{fF} \cdot 0.2 \cdot 3)}} = \sqrt{\frac{270\text{ps}}{22.5\text{ps}}} = 3.46 \approx \underline{3}$$

$$M = \sqrt{\frac{R_{\text{eqn}}}{C_G (1 + \beta)} \frac{C_{\text{int}}}{R_{\text{int}}}} = \sqrt{\frac{12.5\text{k}\Omega}{2\text{fF} \cdot 0.2 \cdot 3} \frac{0.1\text{fF}/\mu\text{m}}{0.054\Omega/\mu\text{m}}}$$

$$= \sqrt{1.042 \times 10^{19} \cdot 1.82 \times 10^{-15}} = 137.7 \approx \underline{140}$$

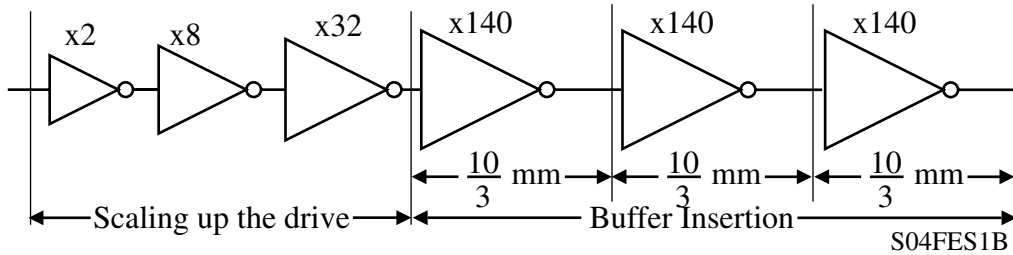
c.) Find the number of cascaded inverters to go from X2 to X140 with a fanout of 4.

$$n = \frac{\ln(C_{\text{load}}/C_{\text{in}})}{\ln f} = \frac{\ln(140/2)}{\ln 4} = 3.06 \approx \underline{3}$$

The design of the inverters driving and insertion buffers is shown below.

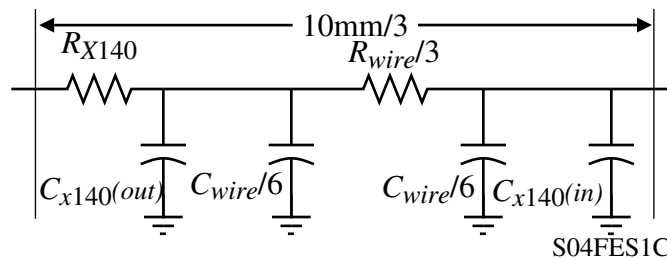
Problem 1 – Continued

c.) Continued.



Note that for the optimum delay, the size of the buffer being driven by the X32 buffer should be X128. However, it has been increased to X140 to be the first insertion buffer. The alternative would be to use a different fanout or add another buffer which would increase the delay. We will assume the above design represents the best choice under the conditions given.

d.) The model one stage of the buffer insertion is given below.



$$R_{X140} = \frac{12.5K}{140} = 90\Omega, \quad C_{X140(out)} = 140(3 \cdot W \cdot C_{self}) = 140 \cdot 3 \cdot 0.4 \cdot 1 = 168\text{fF},$$

$$C_{X140(in)} = 140(3 \cdot W \cdot C_g) = 140 \cdot 3 \cdot 0.4 \cdot 2 = 336\text{fF}, \quad C_{wire} = 1\text{pF}$$

The delay of the buffer insertion stage modeled above is,

$$\tau_{buffer\ insertion+wire/3} = (90)(168\text{fF} + 167\text{fF}) + (90+180)((167\text{fF} + 336\text{fF})) = 166\text{ ps}$$

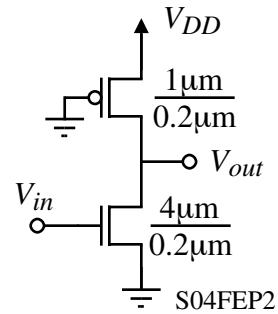
The delay of the design is expressed as

$$\text{Delay} = 3\text{FO4} + 3\left(\text{Buffer} + \frac{\text{Wire}}{3}\right) = 3 \cdot 100\text{ps} + 3(166\text{ps}) = \underline{\underline{798\text{ps} = 0.798\text{ns}}}$$

Problem 2 – (20 points – This problem is optional)

(a.) Estimate the values of t_{PLH} and t_{PHL} for the following pseudo-NMOS inverter that does not have an external load on it (only its own self-capacitance). Assume that a ramp input is applied.

(b.) Usually $t_{PLH} \gg t_{PHL}$ for this type of inverter. Give two reasons why the p-channel device is not made larger so that $t_{PLH} = t_{PHL}$.

Solution

a.)

$$t_{PLH}(\text{step}) = R_p C_{eff} = R_{eqp} \left(\frac{L_p}{W_p} \right) 5 \cdot C_{eff} = 30 \text{k}\Omega (0.2) (5) 1 \text{fF} = 30 \text{ps}$$

$$t_{PHL}(\text{step}) = R_n C_{eff} = R_{eqn} \left(\frac{L_n}{W_n} \right) 5 \cdot C_{eff} = 12.5 \text{k}\Omega \left(\frac{0.2}{4} \right) (5) 1 \text{fF} = 3.125 \text{ps}$$

$$t_{PLH}(\text{ramp}) = 1.5 t_{PLH}(\text{step}) = 1.5(30 \text{ps}) = \underline{45 \text{ps}}$$

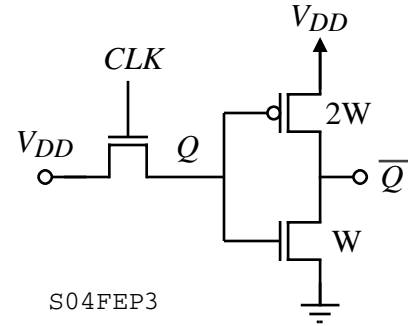
$$t_{PHL}(\text{ramp}) = 1.5 t_{PHL}(\text{step}) = 1.5(3.125 \text{ps}) = \underline{4.69 \text{ps}}$$

b.) Two possible reasons are:

- 1.) Increases V_{OL} .
- 2.) Requires more area.

Problem 3 – (20 points – This problem is optional)

For the dynamic D-latch shown, compute the output voltages at Q and \overline{Q} for the given input when the CLK goes high (V_{DD}). Assume $0.18\mu\text{m}$ CMOS technology, $W = L = 200\text{nm}$, and $V_{DD} = 1.8\text{V}$. Use the velocity saturation models for the transistors.

**Solution**

The first task is to find V_Q which is complicated by the bulk-source voltage not being zero. We know that,

$$V_T = V_{TO} + \gamma\sqrt{V_{SB} + |2\phi_F|} - \gamma\sqrt{|2\phi_F|}$$

$$\text{or } V_Q = 1.8 - V_T = 1.8 - 0.5 - \gamma\sqrt{V_Q + |2\phi_F|} + \gamma\sqrt{|2\phi_F|}$$

$$V_Q = 1.3 - 0.3\sqrt{V_Q + 0.84} + 0.3\sqrt{0.84} = 1.575 - 0.3\sqrt{V_Q + 0.84}$$

Solving by quadratic or iterating gives $\underline{\underline{V_Q = 1.1516\text{V}}}$ $\Rightarrow V_{SG} = 0.6484\text{V}$

We see from this value that the PMOS is saturated and the NMOS is active. Therefore,

$$\frac{2Wv_{sat}C_{ox}(V_{SG} - 0.5)^2}{(V_{SG} - 0.5) + E_cL} = \frac{W}{L} \frac{\mu_e C_{ox}}{\left(1 + \frac{V_Q}{E_cL}\right)} \left[(V_Q - V_{TO}) \overline{V_Q} - \frac{\overline{V_Q}^2}{2} \right]$$

$$\left(1 + \frac{\overline{V_Q}}{1.2}\right) \left(\frac{2(0.2 \times 10^{-4})(8 \times 10^6)(0.648 - 0.5)^2}{(0.148 + 0.5)(270)} \right) = 0.652 \overline{V_Q} - \frac{\overline{V_Q}^2}{2}$$

$$\left(1 + \frac{\overline{V_Q}}{1.2}\right) (0.0259) = 0.652 \overline{V_Q} - \frac{\overline{V_Q}^2}{2} \rightarrow \overline{V_Q}^2 - 1.303 \overline{V_Q} + 0.052 = 0$$

$$\overline{V_Q} = 0.6516 \pm 0.5\sqrt{1.303^2 - 4 \cdot 0.052} = 0.6516 \pm 0.06103 = 41\text{mV}$$

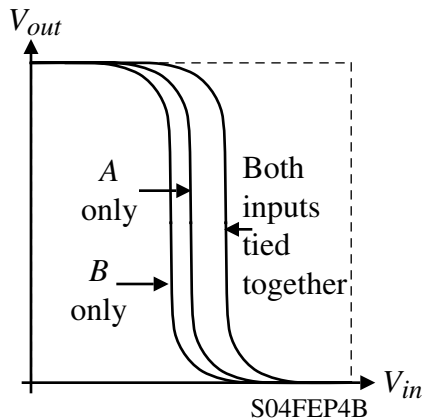
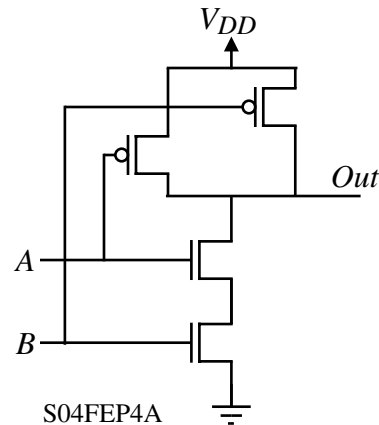
$$\therefore \underline{\underline{\overline{V_Q} = 41\text{mV}}}$$

Problem 4 – (20 points – This problem is optional)

Use 0.18 μm technology for this problem.

(a.) For the NAND gate shown, size the transistors to deliver a switching threshold of $V_S = 0.75\text{V}$. Place the device sizes (W) on the schematic in units of nanometers assuming $L = 200\text{nm}$. Choose the W such that R_{pullup} is the same as the standard inverter.

(b.) The voltage transfer curve of this gate is shown below for various combination of inputs. Provide an explanation as to why this occurs. How would you adjust the expression of V_S to account for this effect?

Solution

$$\text{a.) } V_S = \frac{V_{DD} - |V_{Tp}| + \chi V_{Tn}}{1 + \chi}$$

$$\text{where } \chi = \sqrt{\frac{\mu_n W_n}{\mu_p W_p}}$$

$$0.75 = \frac{1.8 - 0.5 + \chi 0.5}{1 + \chi} \rightarrow 0.75 + 0.75\chi = 1.3 + 0.5\chi$$

$$\therefore 0.25\chi = 0.55 \rightarrow \chi = 2.2$$

$$\chi^2 = \frac{\mu_n W_n}{\mu_p W_p} \rightarrow 2.2^2 = \frac{540 W_n}{180 W_p} \rightarrow \frac{W_n}{W_p} = \frac{180}{540} 2.2^2 = 1.613$$

To get the standard pull-up resistance, W_p must be 400nm. Therefore,

$$\underline{W_p = 400\text{nm}} \text{ and } \underline{W_n = 1.613 \cdot 400\text{nm} = 645\text{nm}}$$

Another way to work this problem is to assume $L_n = L_p = L$. Therefore,

$$\chi = \sqrt{\frac{E_{cp} W_n}{E_{cn} W_p}} = 2 \sqrt{\frac{W_n}{W_p}} = 2.2 \rightarrow \frac{W_n}{W_p} = 1.21$$

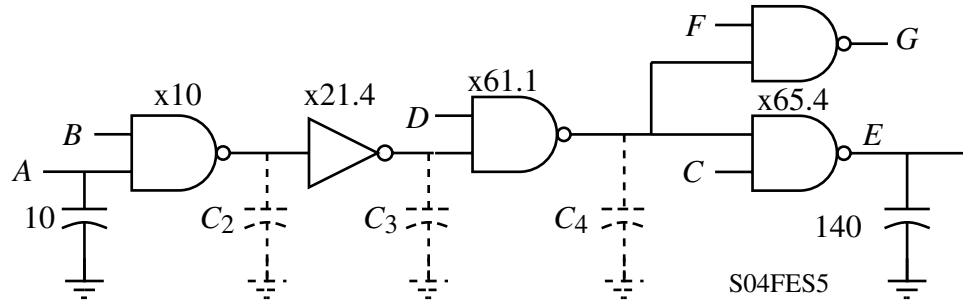
Choosing $W_p = 400\text{nm}$ gives $W_n = 484\text{nm}$ which are acceptable answers although slightly different.

(b.) Compared with B , A moves to the left because of the body effect on the NMOS transistor.

With both inputs tied together the pull-down is weaker because neither input is at V_{DD} initially.

Problem 5 – (20 points – This problem is optional)

What is the minimum possible delay through the following circuit from node *A* to node *E*, and how would you size the gates? You can leave the delay and sizes in unitless quantities. Assume that the two NAND gates at the output are the same size.

Solution

$$LE = (4/3) \quad \times \quad (1) \quad \times \quad (4/3) \quad \times \quad (4/3) = (4/3)^3$$

$$BE = (1) \quad \times \quad (1) \quad \times \quad (1) \quad \times \quad (2) = 2$$

$$FO = \frac{140}{10} = 14$$

$$\therefore PE = (4/3)^3(2)(14) = 66.4 \quad \rightarrow \quad SE = (PE)^{1/4} = 2.854$$

$$C_4 = \frac{140(4/3)}{2.854} = \underline{\underline{65.4}}$$

$$C_3 = \frac{2 \cdot 65.4(4/3)}{2.854} = \underline{\underline{61.1}}$$

$$C_2 = \frac{61.1(1)}{2.854} = \underline{\underline{21.4}}$$

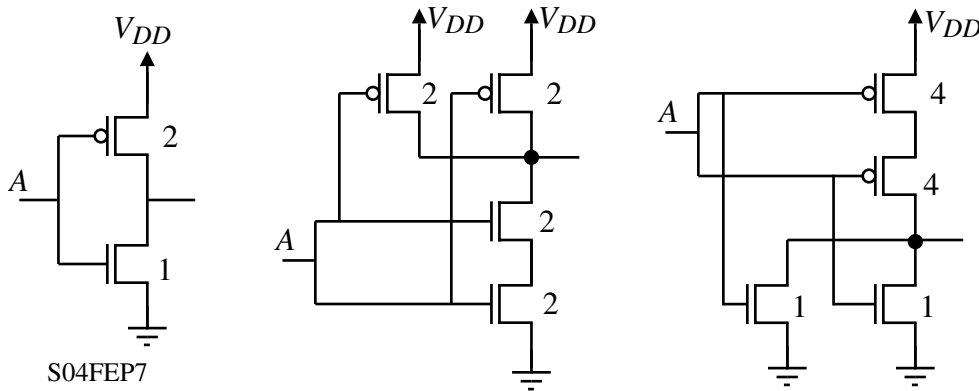
$$C_{in} = \frac{21.4(4/3)}{2.854} = 10$$

$$D = 4(2.854) + 3(1) + (0.5) = \underline{\underline{14.91}}$$

Problem 7 – (20 points – This problem is optional)

(a.) Estimate the worst-case fall propagation delay, t_{PHL} , for the circuits below. Assume that each gate is only loaded by its own self-capacitance and a step function is applied at the inputs. The values beside each transistor are W/L ratios. Identify the fastest and slowest gate given these configurations. Assume that the channel length of all transistors is $0.2\mu\text{m}$.

(b.) Now assume that there is a single 100fF loading of each of the gates above (and the self capacitances are now zero). Compute the t_{PHL} delays for the gates and again identify the fastest and the slowest gates.

Solution

(a.)

Inverter: $\tau = 0.7RC_{inv} = 0.7(12.5\text{k}\Omega)(3)(0.2\mu\text{m})(1\text{fF}/\mu\text{m}) = 5.25\text{ps}$

NAND: $\tau = 0.7RC_{nand} = 0.7(12.5\text{k}\Omega)(8)(0.4\mu\text{m})(1\text{fF}/\mu\text{m}) = 28\text{ps}$

NOR: $\tau = 0.7RC_{nor} = 0.7(12.5\text{k}\Omega/2)(10)(0.4\mu\text{m})(1\text{fF}/\mu\text{m}) = 17.5\text{ps}$

Therefore the inverter is the fastest and the NAND gate the slowest.

(b.)

Inverter: $\tau = 0.7RC_{inv} = 0.7(12.5\text{k}\Omega)(100\text{fF}) = 875\text{ps}$

NAND: $\tau = 0.7RC_{nand} = 0.7(12.5\text{k}\Omega)(100\text{fF}) = 875\text{ps}$

NOR: $\tau = 0.7RC_{nor} = 0.7(12.5\text{k}\Omega/2)(100\text{fF}) = 438\text{ps}$

Therefore the NOR is the fastest and the NAND gate and inverter the slowest.