FINAL EXAMINATION

NAME_____SCORE_____/100

Problem	⓵	2	3	4	5	6	7	Sum
Points								

INSTRUCTIONS: This exam is open textbook only. The exam consists of 7, 20-point problems of which you are to work only 5 for a total of 100 points. Problem 1 must be worked and you may choose any four of the last six problems for a total of five problems. Please circle the number in the table above of the five problems you wish graded. If you do not indicate the problems to be graded, then problems 1 through 5 will be graded regardless of whether they are worked or not. Be sure to turn in only the 5 problems you wish graded in proper numerical order. Please show your work leading to your answers so that maximum partial credit may be given where appropriate.

Problem 1 - (20 points – This problem is required)

a.) An interconnect line is 10 mm long and has a resistance of 54mΩ/μm and a capacitance of 0.1fF/μm and is driven by a 2X inverter (an inverter with an 8λ PMOS and a 4λ NMOS where λ = 0.1μm). What is the total delay of the circuit from the input of the inverter to the end of the interconnect line?

b.) Find the number of buffers (round off to the nearest integer) and the size of these buffers to minimize the delay of the 10 mm interconnect through buffer insertion.

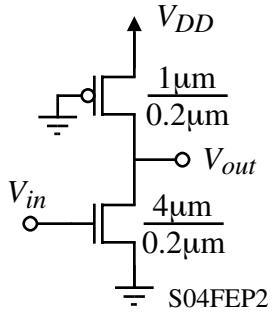
c.) Since the X2 buffer probably cannot drive the insertion buffer at the input directly, use a fanout of 4 (FO4) to design a cascade of inverters that will allow the X2 buffer at the input to drive the first insertion buffer with minimum delay.

d.) For your design above which includes the cascade of inverters at the input followed by the buffer insertion in the 10 mm interconnect, compute the delay value from the 2X inverter at the input to the end of the interconnect. Assume that the average F04 delay of the cascaded inverters is 100ps.

Problem 2 – (20 points – This problem is optional)

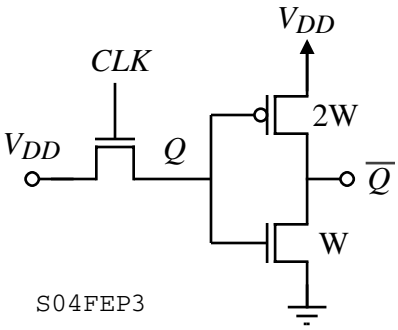
(a.) Estimate the values of t_{PLH} and t_{PHL} for the following pseudo-NMOS inverter that does not have an external load on it (only its own self-capacitance). Assume that a ramp input is applied.

(b.) Usually $t_{PLH} >> t_{PHL}$ for this type of inverter. Give two reasons why the p-channel device is not made larger so that $t_{PLH} = t_{PHL}$.



Problem 3 – (20 points – This problem is optional)

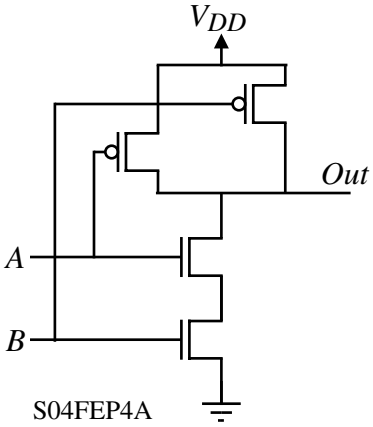
For the dynamic D-latch shown, compute the output voltages at Q and $\overline{Q}$ for the given input when the CLK goes high (V_{DD}). Assume 0.18μm CMOS technology, $W = L = 200$nm, and $V_{DD} = 1.8$V. Use the velocity saturation models for the transistors.



Problem 4 – (20 points – This problem is optional)

Use 0.18μm technology for this problem.

(a.) For the NAND gate shown, size the transistors to deliver a switching threshold of V_S = 0.75V. Place the device sizes (W) on the schematic in units of nanometers assuming L = 200nm. Choose the W such that R_{pullup} is the same as the standard inverter.



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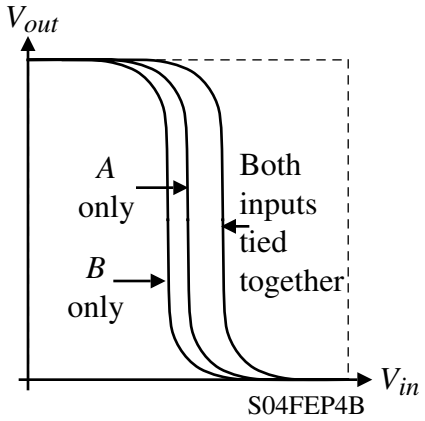
(b.) The voltage transfer curve of this gate is shown below for various combination of inputs. Provide an explanation as to why this occurs. How would you adjust the expression of V_S to account for this effect?



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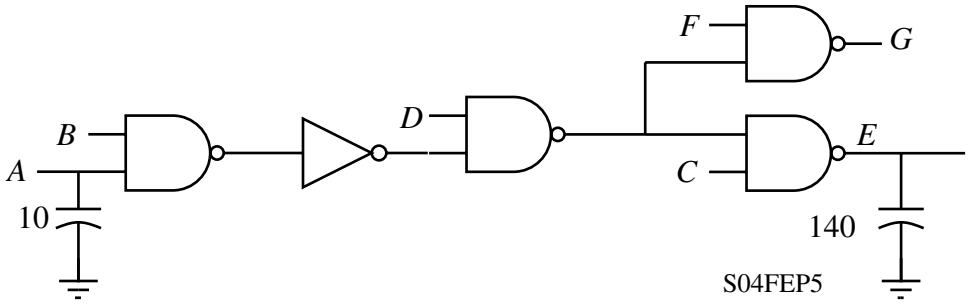
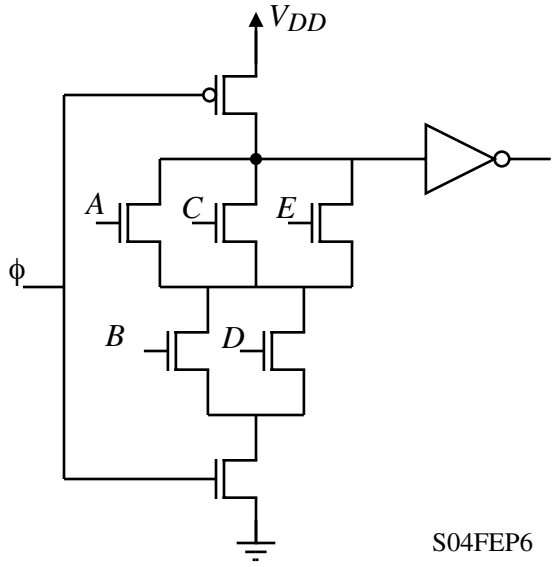
Problem 5 – (20 points – This problem is optional)

What is the minimum possible delay through the following circuit from node *A* to node *E*, and how would you size the gates? You can leave the delay and sizes in unitless quantities. Assume that the two NAND gates at the output are the same size.



Problem 6 – (20 points – This problem is optional)

A dynamic logic gate is shown. The pre-charge device has a W/L of 5, the n-channel devices have a W/L of 3, and inverter has a pull-up of 4 and a pull-down of 1. (a.) What is the logic function of the gate at the output of the inverter? (b.) Why is the output inverter skewed? (c.) Using the device sizes above, what is the logical effort of input *B* of the first stage of the domino logic (when its immediate output is falling), and the inverter (when its output is rising). Computer these two values separately.



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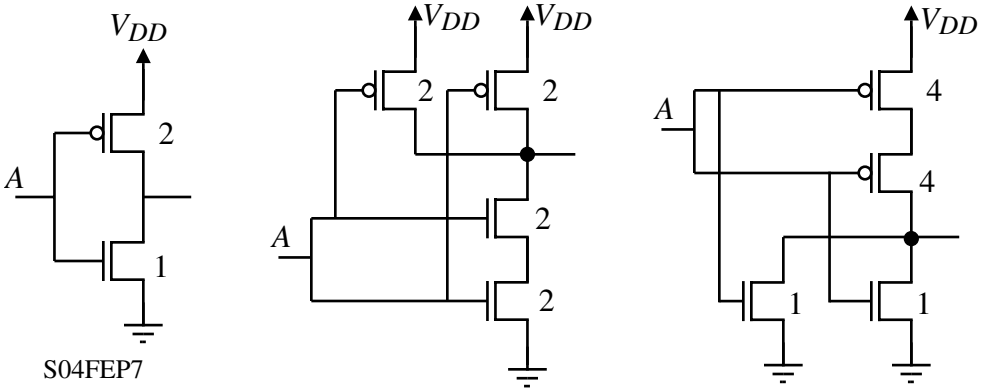
Problem 7 – (20 points – This problem is optional)

(a.) Estimate the worst-case fall propagation delay, t_{PHL}, for the circuits below. Assume that each gate is only loaded by its own self-capacitance and a step function is applied at the inputs. The values beside each transistor are W/L ratios. Identify the fastest and slowest gate given these configurations. Assume that the channel length of all transistors is 0.2μm.

(b.) Now assume that there is a single 100fF loading of each of the gates above (and the self capacitances are now zero). Compute the t_{PHL} delays for the gates and again identify the fastest and the slowest gates.



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Extra sheet of paper.