Homework Assignment No. 1 - Solutions

Problem P1.7

This question **is** as easy as it looks, no tricks here.

    a. The delay from 'a' to 'b' is simply the delay of an inverter times the number of inverters which would be 10 ns.

    b.

        i. The period in this case is simply twice the delay around the loop, T=20 ns.

        ii. The frequency is 1/T =50 MHz.

Problem P1.8

The delay of an RC circuit with a step input applied is:

$$V(t) = 1.2(1 - e^{-t/RC})$$

In our case, we are solving for t:

    c. For V(t)=0.6V:

$$t = 12.5(10^3) \times (100)10^{-15} \ln\left(\frac{1.2}{0.6}\right) = 12.5 \times 10^{-10} \ln(2) = 866ps$$

    d. 1.2V:

$$t = \infty$$

    This circuit will never read 1.2V.

    e. The delay from 10% to 90% V_{DD}:

$$0.1 = (1 - e^{-t/RC})$$
$$\therefore t_{10\%} = 132\,ps$$

$$0.9 = (1 - e^{-t/RC})$$
$$\therefore t_{90\%} = 2.88ns$$

$$t = t_{90\%} - t_{10\%} = 2.88 - 0.132 = 2.75ns$$

Problem P1.9

The delay for f and g uses the exponential rise/fall equation:

    f. For R_{DOWN}:

$$V(t) = 1.2\,e^{-t/RC} \qquad \therefore t_{DOWN} = 8.66ms$$

    g. For R_{UP}:

$$V(t) = 1.2(1 - e^{-t/RC}) \qquad \therefore t_{UP} = 20.8ms$$

    h. The ratio of delays is:

$$t_{RATIO} = \frac{t_{UP}}{t_{DOWN}} = \frac{20.8}{8.7} = 2.4$$

or 0.42 (depending on which way you did the ratio.)

<u>Problem P2.1</u>

P1.2.   a) The solution for the NMOS case is based on Example 2.4:

The equation for V_{T0} is: $V_{T0} = V_{FB} - 2\phi_F - \frac{Q_B}{C_{OX}}$

Calculate each individual component.

$$\phi_{Fp} = \frac{kT}{q}\ln\frac{n_i}{N_A} = -0.026\ln\frac{3\times10^{17}}{1.4\times10^{10}} = -0.44 \ \text{V}$$

$$\phi_{GC} = \phi_{Fp} - \phi_{G(gate)} = -0.44 - 0.55 = -0.99 \ \text{V}$$

$$\varepsilon_{OX} = 4\varepsilon_0 = 3.5\times10^{-13} \ \text{F/cm} \qquad C_{OX} = 1.6\times10^{-6} \ \text{F/cm}^2$$

$$Q_{B0} = 3\times10^{-7} C/cm^2 \qquad \frac{Q_{B0}}{C_{OX}} = \frac{3\times10^{-7}}{1.6\times10^{-6}} = 0.188 \ \text{V}$$

$$\frac{Q_{OX}}{C_{OX}} = \frac{6\times10^{11}\times1.6\times10^{-19}}{1.6\times10^{-6}} = 0.06 \ \text{V}$$

$$V_{TO} = -0.99 - (-0.88) - (-0.188) - 0.060 = +0.018 \ \text{V}$$

For the PMOS device:

$$\phi_{Fn} = \frac{kT}{q}\ln\frac{N_D}{n_i} = 0.026\ln\frac{3\times10^{17}}{1.4\times10^{10}} = 0.44 \ \text{V}$$

$$\phi_{GC} = \phi_{Fn} - \phi_{G(gate)} = 0.44 + 0.55 = +0.99 \ \text{V}$$

$$Q_{B0} = 3\times10^{-7} C/cm^2 \qquad \frac{Q_{B0}}{C_{OX}} = \frac{3\times10^{-7}}{1.6\times10^{-6}} = 0.188 \ \text{V}$$

$$\frac{Q_{OX}}{C_{OX}} = \frac{6\times10^{11}\times1.6\times10^{-19}}{1.6\times10^{-6}} = 0.06 \ \text{V}$$

$$V_{TO} = 0.99 - (0.88) - (0.188) - 0.060 = -0.138 \ \text{V}$$

b) The magnitude of V_{T0} would be higher. Since the device is PMOS this means that V_{T0} is lowered. Since the only thing that's been changed is the doping of the gate, only ϕ_G changes.

The new V_{T0} then becomes:

$$V_{T0} = -0.11 - 0.88 - 0.188 - 0.6 = -1.24\text{V}$$

Problem P2.1 - Continued

c) Since V_{T0} will be adjusted with implanted charge (Q_I):

$$\frac{Q_I}{C_{OX}} = 0.4 - 0.018$$

$$\frac{Q_I}{C_{OX}} = 0.382V$$

$$Q_I = (1.6 \times 10^{-6})(0.382V)$$

To calculate the threshold implant level N_I:

$$qN_I = |Q_I|$$

$$N_I = \frac{|Q_I|}{q}$$

For the NMOS device from part(a):

$$N_I = -\frac{Q_I}{q} = -\frac{0.6 \times 10^{-6}}{1.6 \times 10^{-19}} = 3.82 \times 10^{12} \, ions/cm^2 \text{ (p-type)}$$

For the PMOS device from part(a):

$$N_I = -\frac{Q_I}{q} = -\frac{(1.6 \times 10^{-6})(0.4 - 0.138)}{1.6 \times 10^{-19}} = 2.62 \times 10^{12} \, ions/cm^2 \text{ (n-type)}$$

For the PMOS device from part(b):

$$N_I = -\frac{Q_I}{q} = -\frac{(1.6 \times 10^{-6})(1.24 - 0.4)}{1.6 \times 10^{-19}} = 8.4 \times 10^{12} \, ions/cm^2 \text{ (p-type)}$$

d) The advantage of having the gate doping be n^+ for NMOS and p^+ for PMOS could be seen from analysis above. Doping the gates in such a way leads to devices with lower threshold voltages, but enables the implant adjustment with the same kind of impurities that used in the bulk (p-type for NMOS and n-type for PMOS). If we were to use the same kind of doping in gate as in the body (i.e. n^+ for PMOS and p^+ for NMOS) that would lead to higher un-implanted threshold voltages. Adjusting them to the required lower threshold voltage would necessitate implantation of the impurities of the opposite type near the oxide-Si interface. This is not desirable. Also, the doping of the poly gate can be carried out at the same time as the source and drain and therefore does not require an extra step.
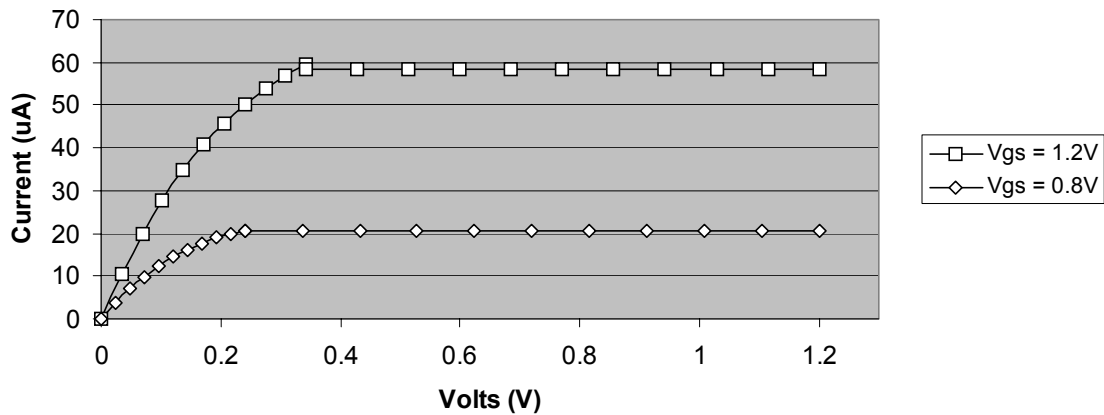
Problem P2.3

P1.3. a)   For each transistor, derive the region of operation. In our case, for $V_{GS} = 0V, 0.4V$, the transistor is in the cutoff region and there is no current. For $V_{GS} = 0.8V, 1.2V$, first calculate the saturation voltage V_{Dsat} using:
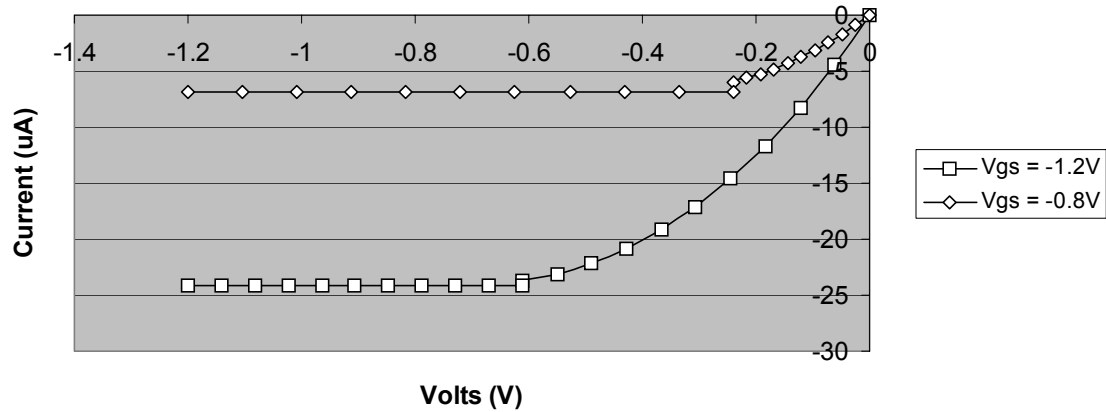
$$V_{DSAT} = \frac{(V_{GS} - V_T)E_C L}{V_{GS} - V_T + E_C L}$$

For our transistors, this would be:

	$V_{GS} = 0.8V$	$V_{GS} = 1.2V$
NMOS	0.24V	0.34V
PMOS	0.35V	0.61V

Next, we derive the IV characteristics using the linear and saturation current equations, we get the graphs shown below.

IV Characteristic of NMOS

Problem P2.3 - Continued

IV Characteristic of PMOS

To plot I_{DS} vs. V_{GS}, first identify the region of operation of the transistor. For $V_{GS} < V_T$, the transistor is in the cutoff region, and there is negligible current. For $V_{GS} > V_T$ and $V_{GS} \leq V_{DS}$, the transistor is in the saturation region and saturation current expression should be used. The graph is shown below. Clearly, it is closer to the linear model.

Ids vs. Vgs of NMOS