Homework No. 5 – Solutions

Problem 1 – P4.10

We will illustrate the process and estimate the solutions for this problem.

We already know that V_{OH}=1.2 V and V_{OL}=0 V. For V_S use:

$$W_N = 0.4um, \quad W_P = 0.8um:$$

$$X = \sqrt{\frac{\frac{W_N}{E_{CN}L_N}}{\frac{W_P}{E_{CP}L_P}}} = \sqrt{\frac{W_N E_{CP}}{W_P E_{CN}}} = \sqrt{\frac{(0.4)(24)}{(0.8)(6)}} = 1.41$$

$$V_S = \frac{0.8 + (0.4)1.41}{1 + 1.41} = 0.566$$

Next V_{IL} and V_{IH} are estimated as follows:

$$V_{IL} = \frac{2V_{out} - V_{DD} - |V_{TP}| + (k_N / k_P)(V_{TN})}{1 + (k_N / k_P)}$$

$$V_{IL} = \frac{2V_{out} - 1.2 - |-0.4| + (2)(0.4)}{1 + (2)} = \frac{2V_{out} - 0.6}{3}$$

We can compute V_{IL} to be roughly 0.533V.

$$V_{IH} = \frac{2V_{out} + V_{TN} + (k_P / k_N)(V_{DD} - |V_{TP}|)}{1 + (k_P / k_N)}$$

$$V_{IH} = \frac{2V_{out} + 0.4 + (2)(1.2 - 0.4)}{1 + (2)} = \frac{2V_{out} + 2}{3}$$

We can compute V_{IH} to be roughly 0.667V.

When we double the size of the PMOS device, the VTC shifts to the right. So V_{IL}, V_S, and V_{IH} will all shift to the right. The recalculation of the switching threshold produces V_S=0.6V.

We can compute V_{IL} to be roughly 0.55V and V_{IH} to be roughly 0.65V.

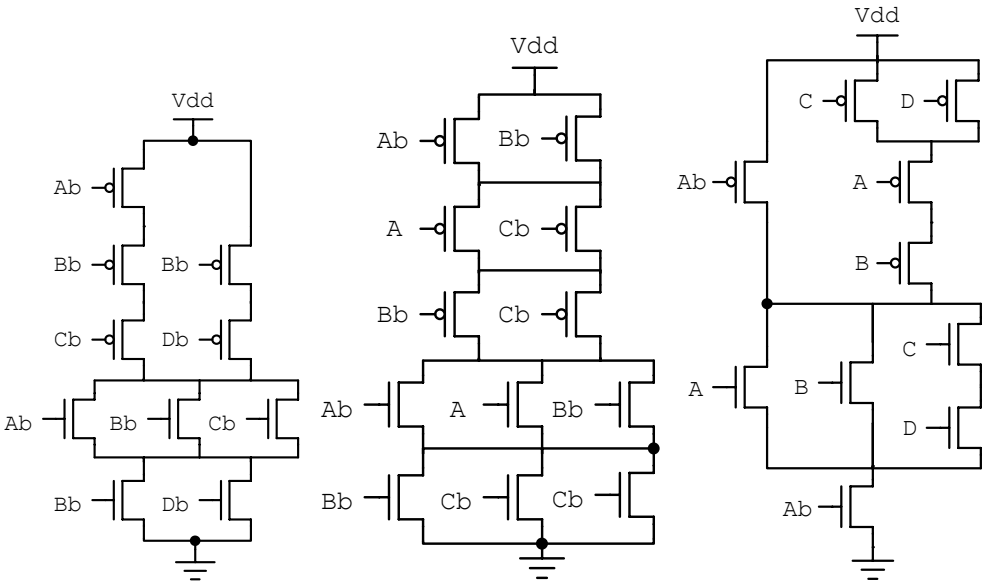
Problem 2 – P5.1

For each problem, restate each Boolean equation into a form such that it can be translated into the p and n-complex of a CMOS gate.

a. $Out = ABC + BD = \overline{\overline{ABC + BD}} = \overline{\left(\overline{A} + \overline{B} + \overline{C}\right)\left(\overline{B} + \overline{D}\right)}$

b. $Out = AB + \overline{A}C + BC = \overline{\overline{AB + \overline{A}C + BC}} = \overline{\left(\overline{A} + \overline{B}\right)\left(A + \overline{C}\right)\left(\overline{B} + \overline{C}\right)}$

c. $Out = \overline{A + B + CD} + A = \overline{A}\,\overline{B}\left(\overline{C} + \overline{D}\right) + A = \overline{\overline{\overline{A + B + CD} + A}} = \overline{\left(A + B + CD\right)\overline{A}}$



Problem 3 – P5.8

The solution is shown below. Notice that there is no relevance with the lengths and widths of the transistors when it comes to V_{OH}, although they the do matter when calculating V_{OL}.

$$V_{out} = V_{GG} - V_T$$

$$V_{GG} = V_{out} + V_{T0} + \gamma\left(\sqrt{V_{out} + 2|\phi_F|} - \sqrt{2|\phi_F|}\right)$$

$$= 1.8 + 0.5 + 0.3\left(\sqrt{1.8 + 0.88} - \sqrt{0.88}\right) = 2.51\text{V}$$

Problem 4 – P5.9

For t_{PLH}, we need to size the pull-up PMOS appropriately.

$$t_{PLH} = 0.7RC = 0.7R_{eqp}\frac{L}{W}C_{LOAD}$$

$$W_p = 0.7R_{SQ}\frac{L}{t_{PLH}}C_{LOAD} = 0.7\left(30k\Omega\right)\frac{\left(2\lambda\right)}{\left(50\times10^{-12}\right)}\left(100\times10^{-15}\right) = 84\lambda$$

For V_{OL}:

$$I_P\left(sat\right) = \frac{W_P v_{sat} C_{OX}\left(V_{GS}-V_T\right)^2}{V_{GS}-V_T+E_{CP}L} = \frac{\left(4.2\times10^{-4}\right)\left(8\times10^{6}\right)\left(1.6\times10^{-6}\right)\left(1.2-0.4\right)^2}{1.2-0.4+\left(24\right)\left(0.1\right)} = 1.08\text{mA}$$

$$I_P\left(sat\right) = \frac{W_N \mu_N C_{OX}\left(V_{OL}-V_{TN}-\frac{V_{OL}}{2}\right)V_{OL}}{L_N\left(1+\frac{V_{OL}}{E_{CN}L}\right)} = \frac{W_N(270)(1.6\times10^{-6})\left(1.2-0.4-\frac{0.1}{2}\right)0.1}{L_N\left(1+\frac{0.1}{0.6}\right)}$$

$$\frac{W_N}{L_N} = 38.5 \quad W_N = 77\lambda \qquad W_3 = 3\times77\lambda = 232\lambda \quad (3\ stack) \quad W_2 = 155\lambda \quad (2\ stack)$$