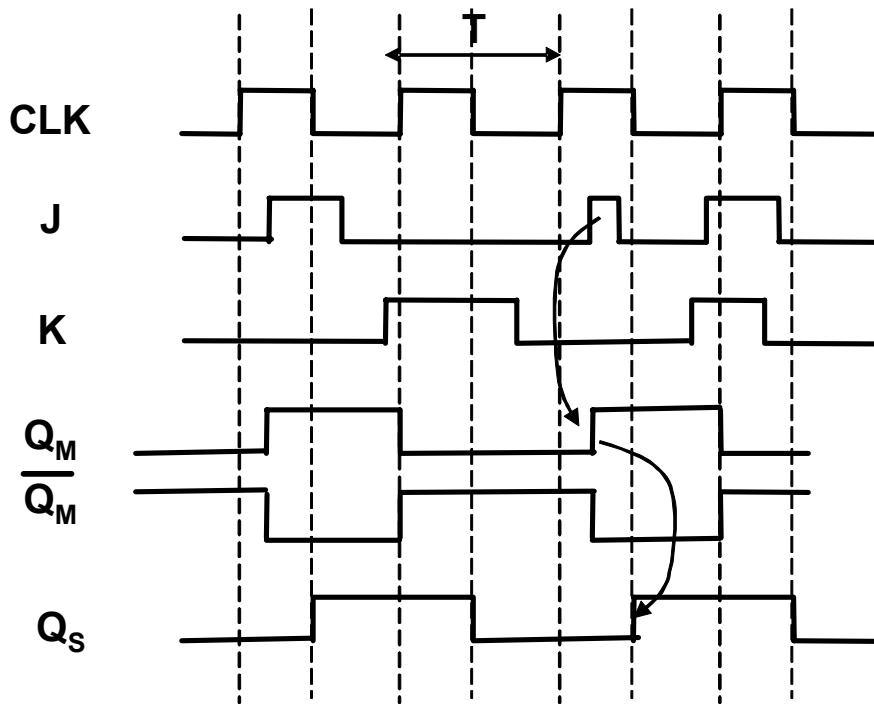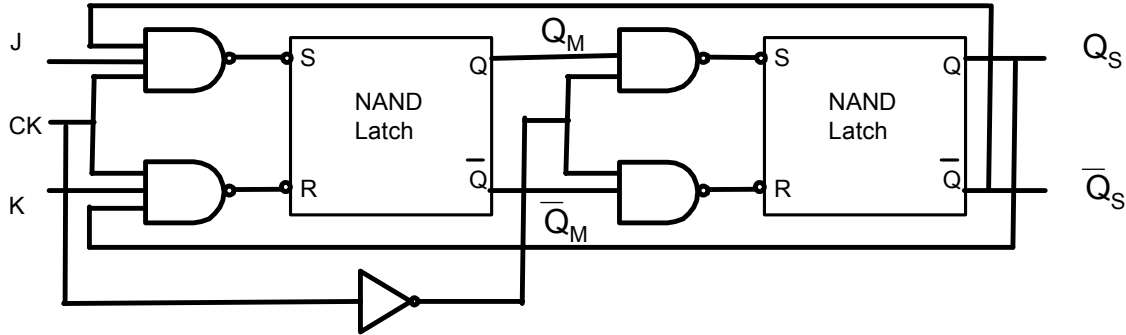## Homework No. 7 – Solutions

Problem 1 – P5.17

P3.1.   The small glitch in J propagates through the flop even though it is small. This is
due to the fact that the JK-flop of Figure 5.20 has the 1's catching problem.

1's catching

Problem 2 – P5.18

The small glitch in J does not propagate through the flop since the edge-triggered configuration does not have a 1's catching problem.

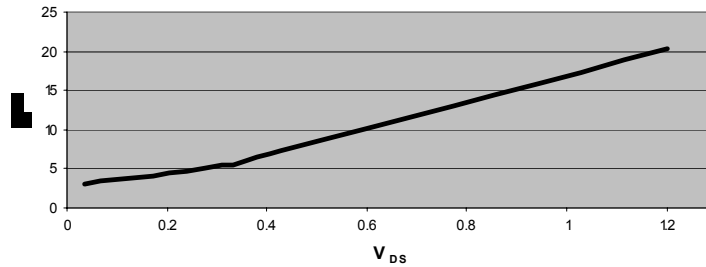

No 1's catching
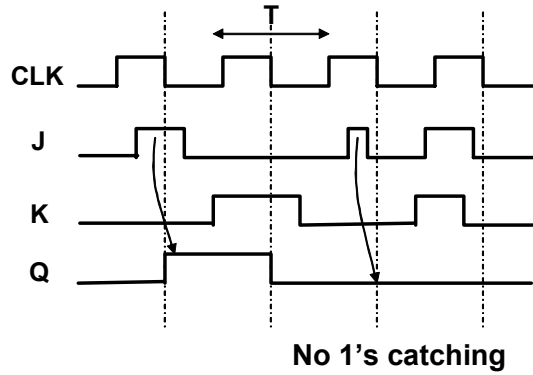
Problem 3 – P6.1

The on-resistance of a unit-sized NMOS device.

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On-resistance of a unit-sized NMOS device

The average on-resistance is approximately 15kΩ. The expression for the average resistance value between V_{DD} and $\frac{V_{DD}}{2}$.

$$R_{ON} = \frac{R_{ON}(V_{DD}) + R_{ON}\left(\frac{V_{DD}}{2}\right)}{2} = \frac{\frac{V_{DS}(V_{DD})}{I_{DS}(V_{DD})} + \frac{V_{DS}\left(\frac{V_{DD}}{2}\right)}{I_{DS}\left(\frac{V_{DD}}{2}\right)}}{2} = \frac{\frac{V_{DD}}{I_{D,sat}} + \frac{\frac{V_{DD}}{2}}{I_{D,sat}}}{2}$$

$$= \frac{3V_{DD}}{4I_{D,sat}} = \frac{3V_{DD}(V_{GS} - V_T + E_{CN}L_N)}{4Wv_{sat}C_{ox}(V_{GS} - V_T)^2}$$

Problem 4 – P6.2

For this case, we will be comparing to SPICE so use L=0.13um. Since the signal must go around the ring twice for one oscillation, the period is :

$$t_{TOT} = N\left(t_{PLH} + t_{PHL}\right) = N\left(R_P C_{LOAD} + R_N C_{LOAD}\right) = N\left(R_P + R_N\right)\left(C_W W\right)$$

$$= N\left(R_{EQP}\frac{L}{W_P} + R_{EQN}\frac{L}{W_N}\right)\left(C_g + C_{eff}\right)\left(W_P + W_N\right)$$

$$= 7\left[\left(30\times10^3\right)\frac{1}{2} + \left(12.5\times10^3\right)\right]\left(2+1\right)\left(10^{-15}\right)\left(0.4\right)$$

$$= 7\left(27.5\times10^3\right)\left(3\times10^{-15}\right)\left(0.4\right) = 231ps$$

$$f = \frac{1}{t_{TOT}} = \frac{1}{231ps} = 4.3\text{GHz}$$

This is independent of inverter size. Consider the delay equation given above which is in terms of W. Since each inverter drives an identical inverter, when we increase the W of an inverter, it acts to reduce the resistance of the driver and increase the capacitance of the load by the same amount (roughly speaking, of course). Therefore, the oscillation frequency should remain constant as we increase the sizes.

The SPICE results show a period of about 250ps or a frequency of 4GHz.
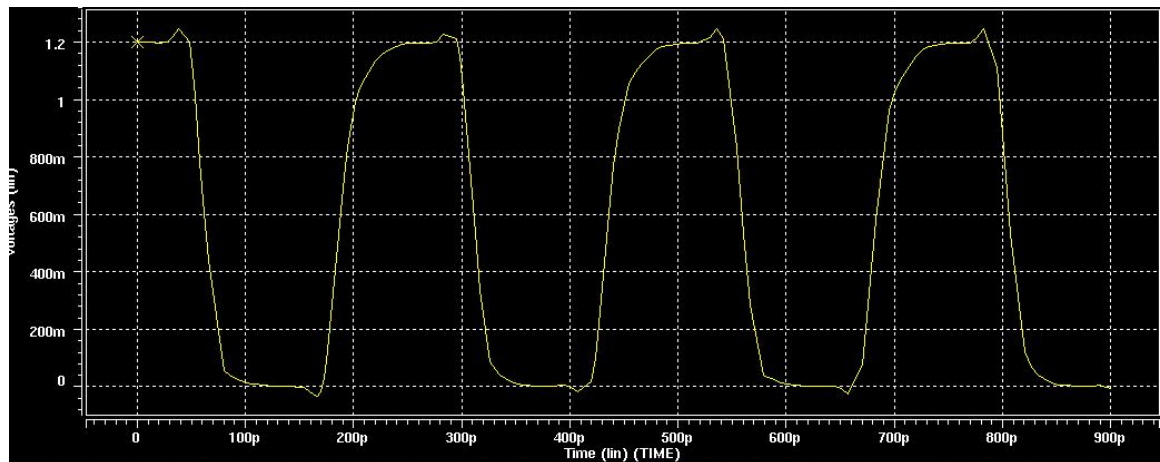
Problem 4 – P6.4

The self-capacitance in these cases are the capacitances that will make the transition from 0 to V_{DD} or vice versa.

    a. In this case, all the internal nodes will be charged so the self-capacitance is :

$$C_{SELF} = C_{eff}\left(2W + 2W + 3W + 3W + 3W\right) = 13C_{eff}W$$

    b. In this case, all the internal nodes but the one above the bottom NMOS transistor will be charged:

$$C_{SELF} = C_{eff}\left(2W + 2W + 3W + 3W\right) = 10C_{eff}W$$

    c. If we assume a worst-case scenario, this node will be charged up to V_{DD} from 0.

$$C_{SELF} = C_{eff}\left(2W + 2W + 3W + 3W + 3W\right) = 13C_{eff}W$$

    d. The node above the bottom-most NMOS transistor has already been discharged.

$$C_{SELF} = C_{eff}\left(2W + 2W + 3W + 3W\right) = 10C_{eff}W$$