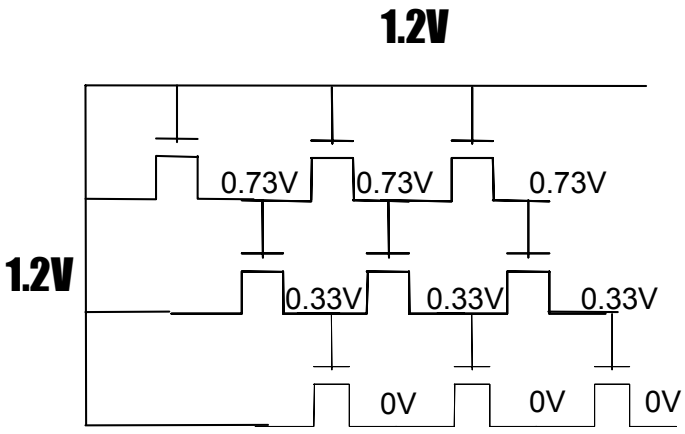
Homework No. 9 – Solutions

Problem 1 – P7.1

Assume that all nodes start at 0V. The first row outputs will be at $V_{DD} - V_T$. Since these nodes are also the gate nodes of the second row of transistors, their source nodes will be at $V_{DD} - 2V_T$. Likewise, the last row of transistors have voltages of $V_{DD} - 3V_T$. However, this value is below 0V so we leave them at 0V.



Problem 2 – P7.2

(a)

A	B	Out
0	0	Z
0	1	1
1	0	Z
1	1	Z

(b.)

A	B	Out
0	0	1
0	1	1
1	0	0
1	1	1

(c)

A	B	C	Out
0	0	0	Z
0	0	1	Z
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	Z
1	1	0	0
1	1	1	Z

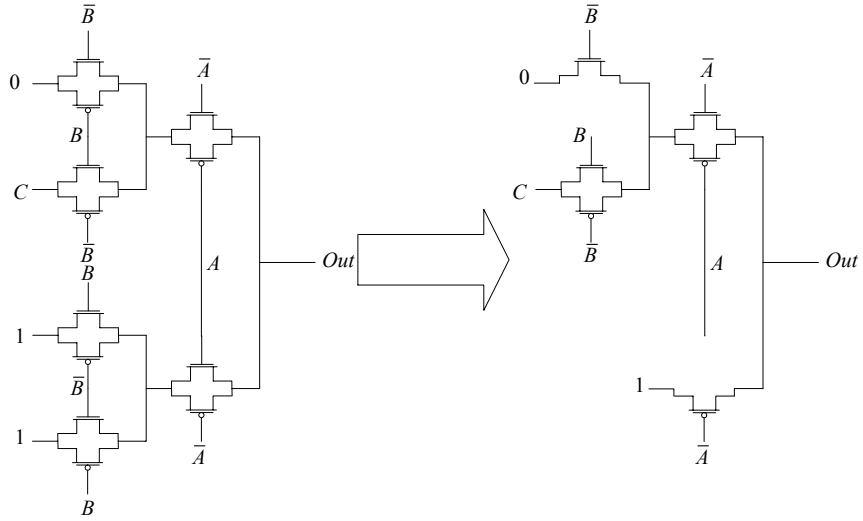
(d)

A	B	C	Out
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

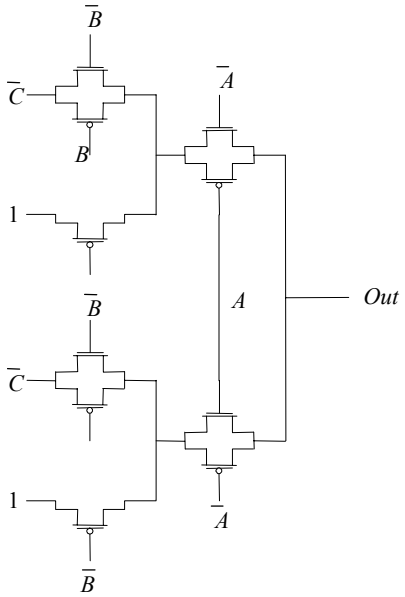
Problem 3 – P7.4

(a) $Out = A + BC$

A	B	C	Out
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1



(b) $Out = AB + BC + \overline{C}$



A	B	C	Out
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

Problem 4 – P7.5

(a) $Out = \overline{(A+B)C}$ (b) $Out = \overline{(A+B)(C+D+E)}$