Homework No. 10 – Solutions

Problem 1 – P7.6(a) and (c)
(a.) \( \text{Out} = \overline{A} + \overline{B}C \)

(c.) \( \text{Out} = (\overline{A} + \overline{B} + C) + A\overline{B} = AB\overline{C} + A\overline{B} \)

Problem 2 – P7.7
P3.1. Assuming that one of the transistors in each transmission gate is being driven by a min-sized inverter:

(a.) \( LE = \frac{RC_{pass}}{RC_{inv}} = \frac{(R + R)(1)}{(R)(3)} = \frac{2\mathcal{X}}{3\mathcal{X}} = \frac{2}{3} \)
\( LE_A = \frac{RC_A}{RC_{inv}} = \frac{(3R)(1)}{(R)(3)} = \frac{3\mathcal{X}}{3\mathcal{X}} = 1 \)

(b.) \( LE = \frac{RC_{pass}}{RC_{inv}} = \frac{(3R)(1)}{(R)(3)} = \frac{3\mathcal{X}}{3\mathcal{X}} = 1 \)
\( LE_B = \frac{RC_B}{RC_{inv}} = \frac{(3R)(3)}{(R)(3)} = \frac{9\mathcal{X}}{3\mathcal{X}} = 3 \)
\( LE_C = \frac{RC_C}{RC_{inv}} = \frac{(3R)(1)}{(R)(3)} = \frac{3\mathcal{X}}{3\mathcal{X}} = 1 \)
Problem 3 – P7.10

P3.2. We will use 0.18um technology and the node names below:

For the two inverter inputs:
\[ C_{inv} = C_g \left( 3W \right) = 2(3)(0.2) = 1.2 \text{fF} \]

For the pass gate inputs:
\[ C_{pass} = C_g \left( W \right) = 0.4 \text{fF} \]

At node x:
\[ C_x = C_{eff} \left( 3W \right) + C_{eff} \left( 2W \right) + C_g \left( W \right) = 1.4 \text{fF} \]

At node y:
\[ C_y = 2(C_{eff} \left( 2W \right) + C_g \left( W \right)) + C_{eff} \left( 2W \right) = 2 \text{fF} \]

At node Out:
\[ C_{out} = (C_{eff} \left( 2W \right) + C_g \left( W \right)) + C_{eff} \left( 2W \right) = 1.2 \text{fF} \]

The shortest path is through the one of the \( G_{ND} \) input nodes to the output:
\[ t_{min} = RC_x + 2RC_{out} = \left( 12.5k \right) \left( 1.4fF \right) + 2 \left( 12.5k \right) \left( 1.2fF \right) = 47.5 \text{ps} \]

The longest path is through one of the inverters to the output.
\[ t_{max} = RC_x + 2RC_y + 3RC_{out} = \left( 12.5k \right) \left( 1.4fF \right) + 2 \left( 12.5k \right) \left( 2fF \right) + 3 \left( 12.5k \right) \left( 1.2fF \right) = 112.5 \text{ps} \]
Problem 4 – P7.13

(a.) The input settings that give you the worst-case charge sharing are any of \( a = c = e = 1 \) and both of \( b = d = 0 \). Essentially, what you are doing is trying to create the greatest amount of parasitic capacitances without creating a path to \( G_{ND} \).

(b.) Assuming that transistors share nodes to reduce capacitance.

\[
C_1 = C_g(5W) + C_d(3W) + C_g(5W) = 5.2\,\text{fF}
\]
\[
C_2 = C_d(3W + 3W + 3W) = (1)(9)(0.2) = 1.8\,\text{fF}
\]
\[
V^* = \frac{CV_1}{C_1 + C_2} = \frac{(5.2)(1.8)}{5.2 + 1.8} = 1.34\,\text{V}
\]

The actual voltage would be larger than this since the internal node cannot rise above \( V_{DD} - V_T \).

(c.) This circuit fails if the worst case voltage falls below the switching voltage which can be computed to be \( V_S = 0.92\,\text{V} \). Therefore, the circuit will operate properly.