## Homework No. 10 - Solutions

Problem 1 - P7.6(a) and (c)
(a.) Out $=\bar{A}+\bar{B} C$

(c.) Out $=\overline{(\bar{A}+\bar{B}+C)}+A \bar{B}=A B \bar{C}+A \bar{B}$


Problem 2-P7.7
P3.1. Assuming that one of the transistors in each transmission gate is being driven by a min-sized inverter:
(a.) $L E=\frac{R C_{\text {pass }}}{R C_{\text {inv }}}=\frac{(R+R)(1)}{(R)(3)}=\frac{2 \not K}{3 \not K}=\frac{2}{3}$
$\begin{aligned} L E_{A} & =\frac{R C_{A}}{R C_{i n v}}=\frac{(3 R)(1)}{(R)(3)}=\frac{3 \not K}{3 \not K K}=1 \\ \text { (b.) } & L E_{B}=\frac{R C_{B}}{R C_{i n v}}=\frac{(3 R)(3)}{(R)(3)}=\frac{9 \nsubseteq K}{3 \not C_{C}}=3 \\ R C_{i n v} & =\frac{(3 R)(1)}{(R)(3)}=\frac{3 \not K}{3 \not K K}=1\end{aligned}$

Problem 3-P7. 10
P3.2. We will use 0.18 um technology and the node names below:


For the two inverter inputs:

$$
C_{i n v}=C_{g}(3 W)=2(3)(0.2)=1.2 \mathrm{fF}
$$

For the pass gate inputs:

$$
C_{p a s s}=C_{g}(W)=0.4 \mathrm{fF}
$$

At node x:

$$
C_{x}=C_{e f f}(3 W)+C_{e f f}(2 W)+C_{g}(W)=1.4 f F
$$

At node $y$ :

$$
C_{y}=2\left(C_{e f f}(2 W)+C_{g}(W)\right)+C_{e f f}(2 W)=2 f F
$$

At node Out:

$$
C_{o u t}=\left(C_{e f f}(2 W)+C_{g}(W)\right)+C_{e f f}(2 W)=1.2 f F
$$

The shortest path is through the one of the $G_{N D}$ input nodes to the output:

$$
t_{\min }=R C_{x}+2 R C_{\text {out }}=(12.5 k)(1.4 f F)+2(12.5 k)(1.2 f F)=47.5 \mathrm{ps}
$$

The longest path is through one of the inverters to the output.

$$
t_{\max }=R C_{x}+2 R C_{y}+3 R C_{\text {out }}=(12.5 k)(1.4 f F)+2(12.5 k)(2 f F)+3(12.5 k)(1.2 f F)=112.5 p \mathrm{~s}
$$

## Problem 4 - P7. 13

(a.) The input settings that give you the worst-case charge sharing are any of $a=c=e=1$ and both of $b=d=0$. Essentially, what you are doing it trying to create the greatest amount of parasitic capacitances without creating a path to $G_{N D}$.
(b.) Assuming that transistors share nodes to reduce capacitance.

$$
\begin{aligned}
& C_{1}=C_{g}(5 W)+C_{d}(3 W)+C_{g}(5 W)=5.2 \mathrm{fF} \\
& C_{2}=C_{d}(3 W+3 W+3 W)=(1)(9)(0.2)=1.8 \mathrm{fF} \\
& V^{*}=\frac{C_{1} V_{1}}{C_{1}+C_{2}}=\frac{(5.2)(1.8)}{5.2+1.8}=1.34 \mathrm{~V}
\end{aligned}
$$

The actual voltage would be larger than this since the internal node cannot rise above $\mathrm{V}_{\mathrm{DD}}-\mathrm{V}_{\mathrm{T}}$.
(c.) This circuit fails if the worse case voltage falls below the switching voltage which can be computed to be $\mathrm{V}_{\mathrm{S}}=0.92 \mathrm{~V}$. Therefore, the circuit will operate properly.

