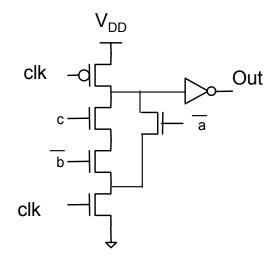
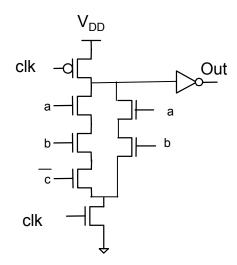
Homework No. 10 – Solutions

Problem 1 - P7.6(a) and (c)

(a.)
$$Out = \overline{A} + \overline{B}C$$



(c.)
$$Out = \overline{(\overline{A} + \overline{B} + C)} + A\overline{B} = AB\overline{C} + A\overline{B}$$



Problem 2 - P7.7

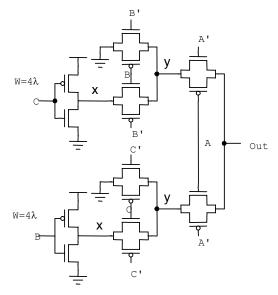
P3.1. Assuming that one of the transistors in each transmission gate is being driven by a min-sized inverter:

(a.)
$$LE = \frac{RC_{pass}}{RC_{inv}} = \frac{(R+R)(1)}{(R)(3)} = \frac{2\cancel{K}}{3\cancel{K}} = \frac{2}{3}$$

(b.) $LE_A = \frac{RC_A}{RC_{inv}} = \frac{(3R)(1)}{(R)(3)} = \frac{3\cancel{K}}{3\cancel{K}} = 1$
 $LE_C = \frac{RC_C}{RC_{inv}} = \frac{(3R)(1)}{(R)(3)} = \frac{3\cancel{K}}{3\cancel{K}} = 1$
 $LE_B = \frac{RC_B}{RC_{inv}} = \frac{(3R)(3)}{(R)(3)} = \frac{9\cancel{K}}{3\cancel{K}} = 3$

<u>Problem 3 – P7.10</u>

P3.2. We will use 0.18um technology and the node names below:



For the two inverter inputs:

$$C_{inv} = C_g (3W) = 2(3)(0.2) = 1.2 \text{fF}$$

For the pass gate inputs:

$$C_{pass} = C_g(W) = 0.4 \text{fF}$$

At node x:

$$C_x = C_{eff}(3W) + C_{eff}(2W) + C_g(W) = 1.4 fF$$

At node y:

$$C_v = 2(C_{eff}(2W) + C_g(W)) + C_{eff}(2W) = 2fF$$

At node Out:

$$C_{out} = (C_{eff}(2W) + C_g(W)) + C_{eff}(2W) = 1.2 fF$$

The shortest path is through the one of the G_{ND} input nodes to the output:

$$t_{\min} = RC_x + 2RC_{out} = (12.5k)(1.4fF) + 2(12.5k)(1.2fF) = 47.5 ps$$

The longest path is through one of the inverters to the output.

$$t_{\text{max}} = RC_x + 2RC_y + 3RC_{out} = (12.5k)(1.4fF) + 2(12.5k)(2fF) + 3(12.5k)(1.2fF) = 112.5ps$$

Problem 4 – P7.13

- (a.) The input settings that give you the worst-case charge sharing are any of a = c = e = 1 and both of b = d = 0. Essentially, what you are doing it trying to create the greatest amount of parasitic capacitances without creating a path to G_{ND} .
- (b.) Assuming that transistors share nodes to reduce capacitance.

$$C_1 = C_g (5W) + C_d (3W) + C_g (5W) = 5.2 \text{fF}$$

$$C_2 = C_d (3W + 3W + 3W) = (1)(9)(0.2) = 1.8 \text{fF}$$

$$V^* = \frac{C_1 V_1}{C_1 + C_2} = \frac{(5.2)(1.8)}{5.2 + 1.8} = 1.34 \text{V}$$

The actual voltage would be larger than this since the internal node cannot rise above V_{DD} - V_{T} .

(c.) This circuit fails if the worse case voltage falls below the switching voltage which can be computed to be V_S =0.92V. Therefore, the circuit will operate properly.