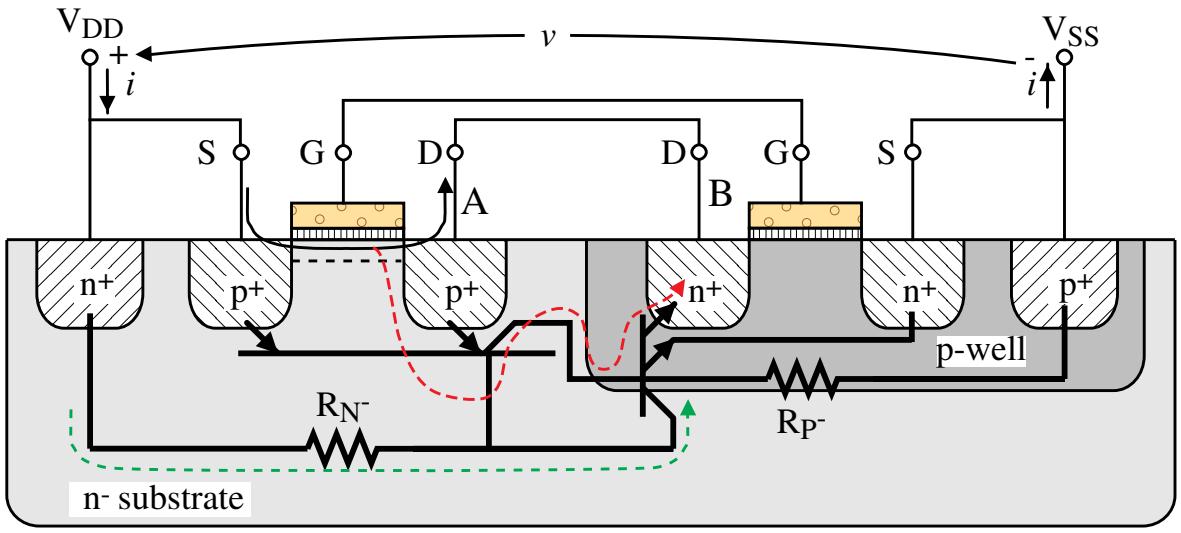
Latch-up in CMOS Technology

Latch-up Mechanisms:

1. SCR regenerative switching action.
2. Secondary breakdown.
3. Sustaining voltage breakdown.

Parasitic lateral PNP and vertical NPN BJTs in a p-well CMOS technology:



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Equivalent circuit of the SCR formed from the parasitic BJTs:

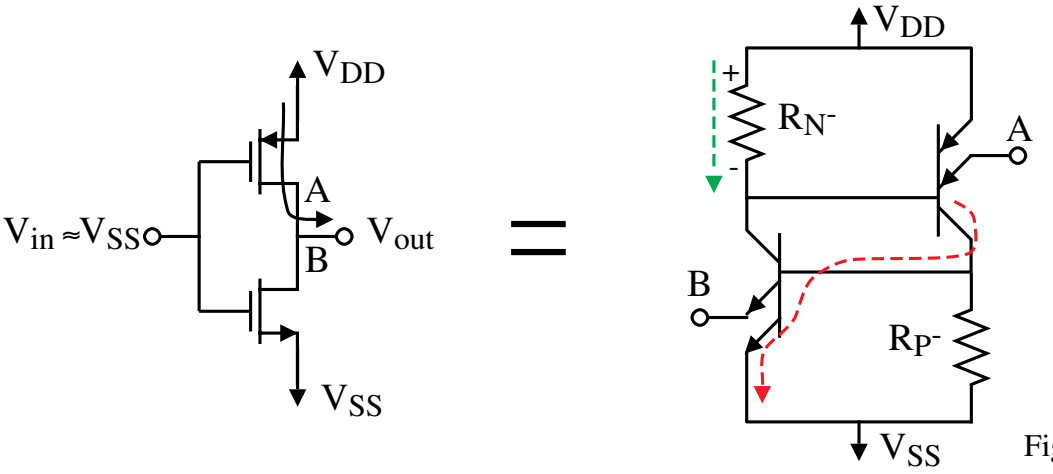

Fig. 190-09

Preventing Latch-Up in a P-Well Technology

1.) Keep the source/drain of the MOS device not in the well as far away from the well as possible. This will lower the value of the BJT betas.

2.) Reduce the values of R_{N-} and R_{P-}. This requires more current before latch-up can occur.

3.) Make a p^- diffusion around the p-well. This shorts the collector of Q1 to ground.

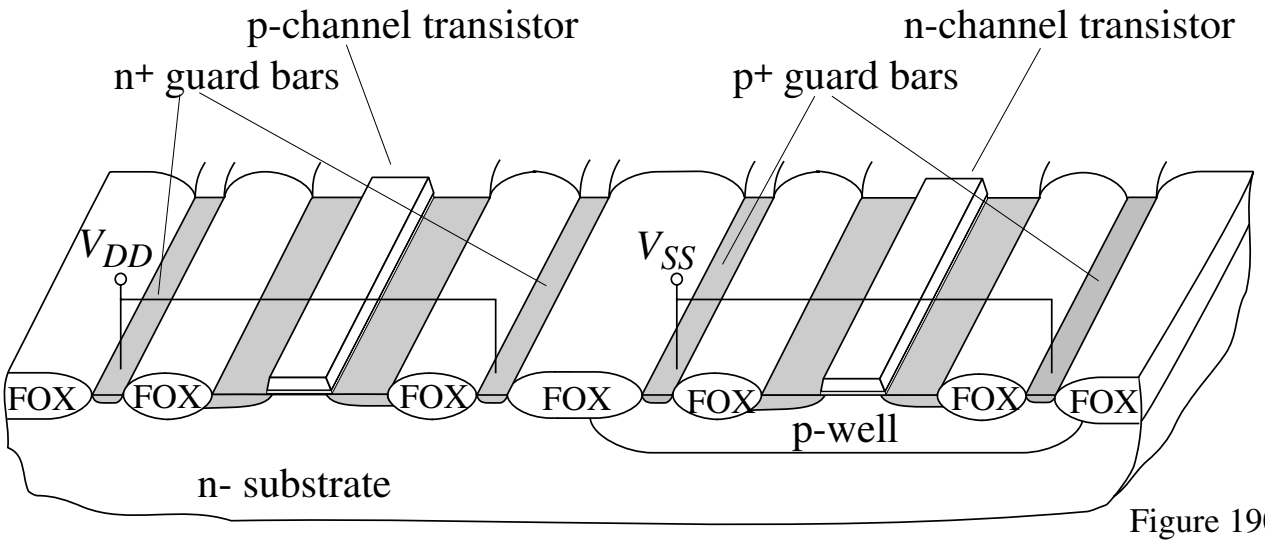

Figure 190-1(

For more information see R. Troutman, "CMOS Latchup", Kluwer Academic Publishers.