Homework #3 will require considerable SPICE usage plus down loading the BSIM3 model so do not wait until the last minute to work on this assignment.

A good way to check the influence of technology variation is to simulate the circuit over temperature.

Temperature Effects

1.) Mobility (KP): $\mu(T) = \mu_0 \left(\frac{T}{300°K}\right)^{-1.5} \rightarrow \mu(T) = \mu_0 \left(\frac{T}{T_0}\right)^{-1.5}$

$\mu_0 = \mu(T_0) = \mu(300°K)$

2.) Threshold (VTO):

$$V_T(T) \approx V_T(T_0) + \alpha(T - T_0) + \cdots\cdots$$

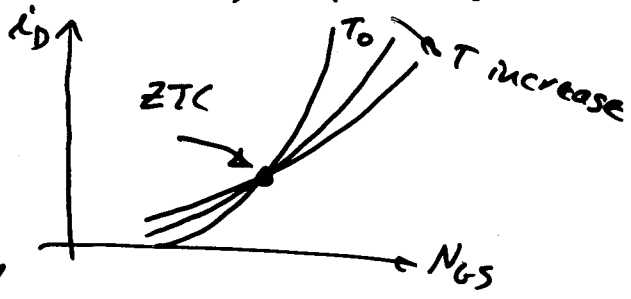
$\alpha = -2\frac{mV}{°}$ to $-3\frac{mV}{°}$ for NMOS

Fact:

$$i_D(T) = \mu_0 \left(\frac{T}{300°K}\right) \frac{C_{ox}}{2} \frac{W}{L} \left[V_{GS} - V_T(T_0) - \alpha(T - T_0)\right]^2$$

A zero temp. coeff. exists for a given value of V_{GS}.

$T \uparrow \rightarrow KP \downarrow \Rightarrow I_D \downarrow$, $V_T \downarrow \Rightarrow I_D \uparrow$



3.) Subthreshold

Since the current is controlled by the minority carrier concentration which is strongly dependent on n_i, then

$$n_i(T) = 1.45 \times 10^{16} \left(\frac{T}{300°K}\right)^{1.5} \exp\left[\frac{1.12}{0.0516} - \frac{E_g(T)}{2\frac{kT}{q}}\right]$$

$\therefore\ I_D(T) \propto T$

Voltage Limitations

1.) Hot carrier effect:

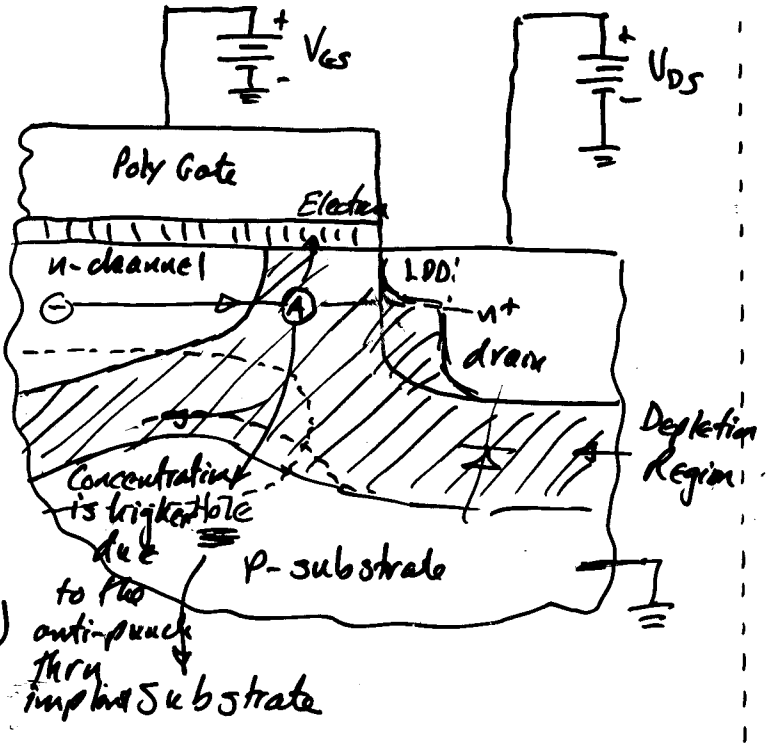
LDD reduce the electric field which in turn reduces HCE.

2.) Voltage Breakdown

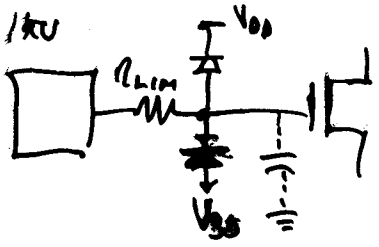
a.) pn junction

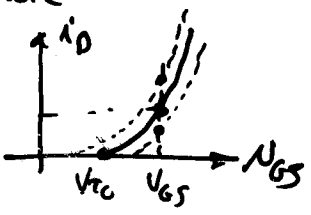
b.) Punch through

(Anti-punch through)

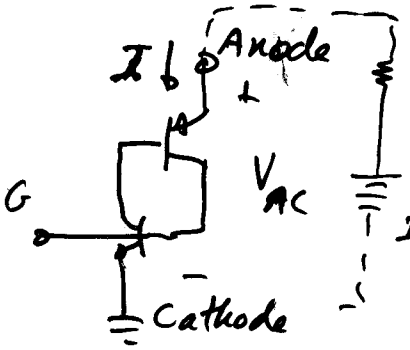


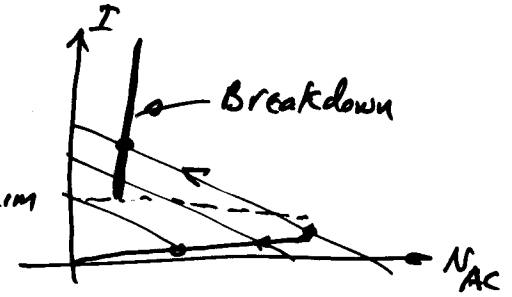
ESD protection:





Silicon-Controlled Rectifier (SCR)





CHAPTER 4 - MOS INVERTER - INTRO & DEFINITIONS

Inverter Symbol 

Types of inverters -

1.) Static
- All nodes have a dc path to ground or to V_{DD}.
- If clocks are used, they are applied to the logic inputs

2.) Dynamic
- Requires periodic clocks synchronized with data signals
- Clocks are applied to the load elements and to transfer gates.