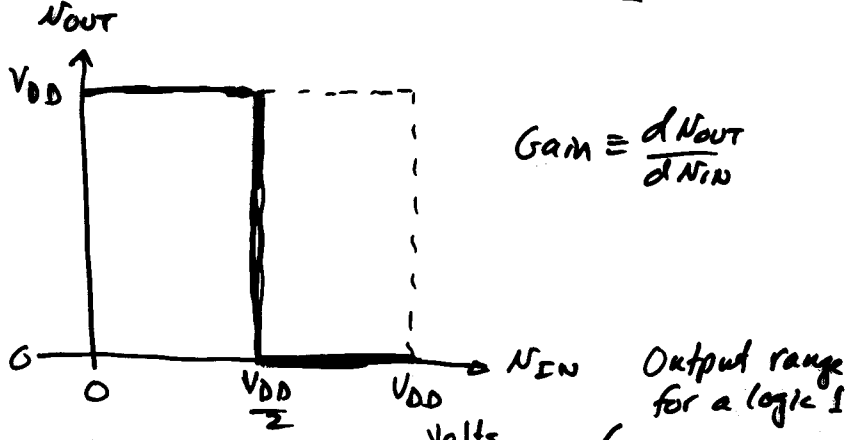
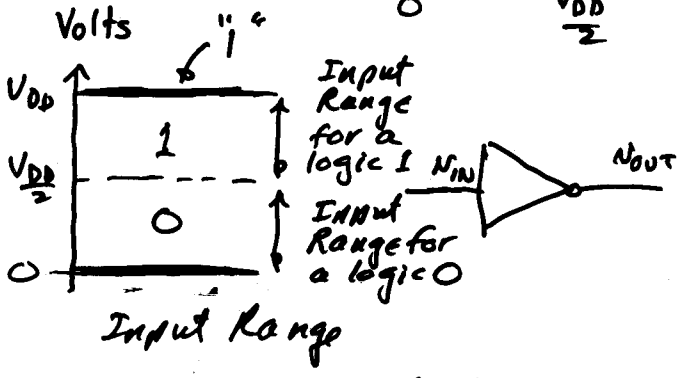
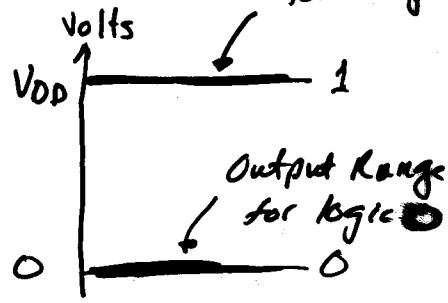
Voltage Transfer Characteristic of an Inverter

Ideal:

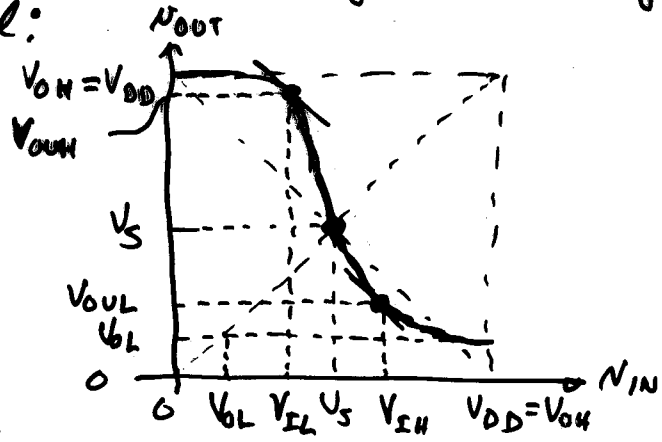


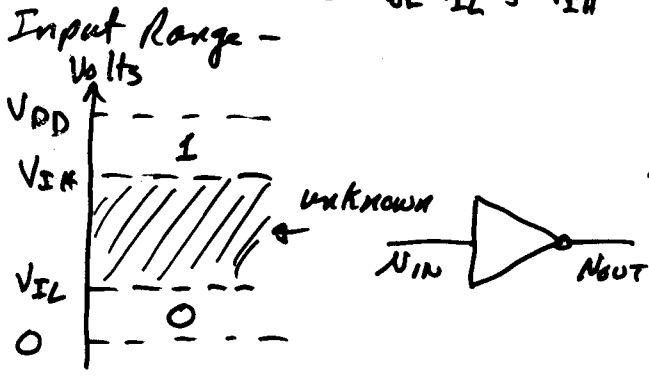


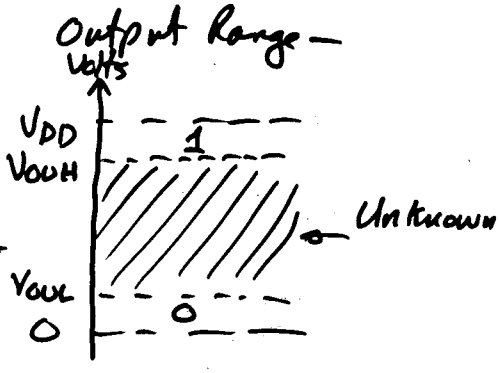


Output range < Input Range

Practical:







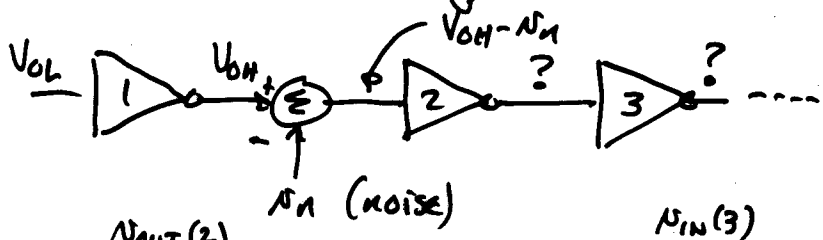
Noise Margin Definitions

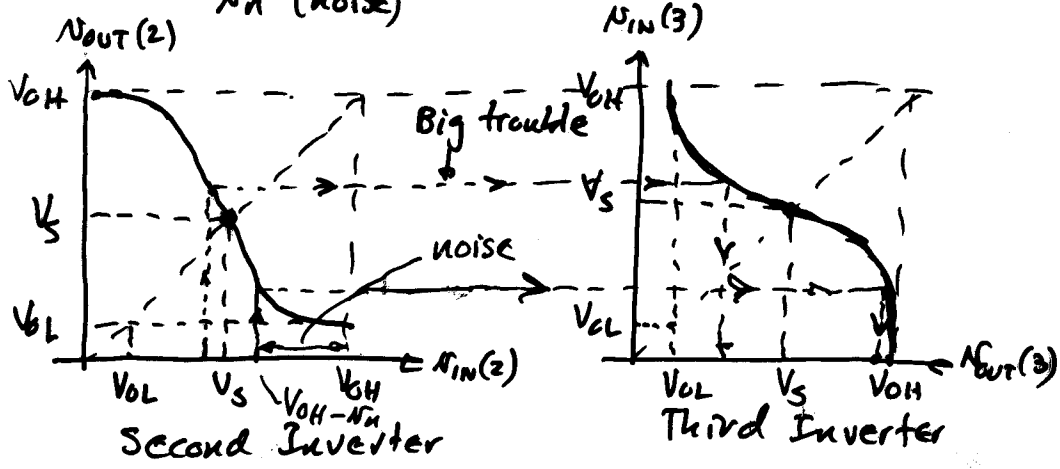
Noise ≡ Unwanted variations of voltages or currents at the logic nodes.

Noise Margin (NM) ≡ largest value of noise at the input that will be attenuated as it passes from input to output.

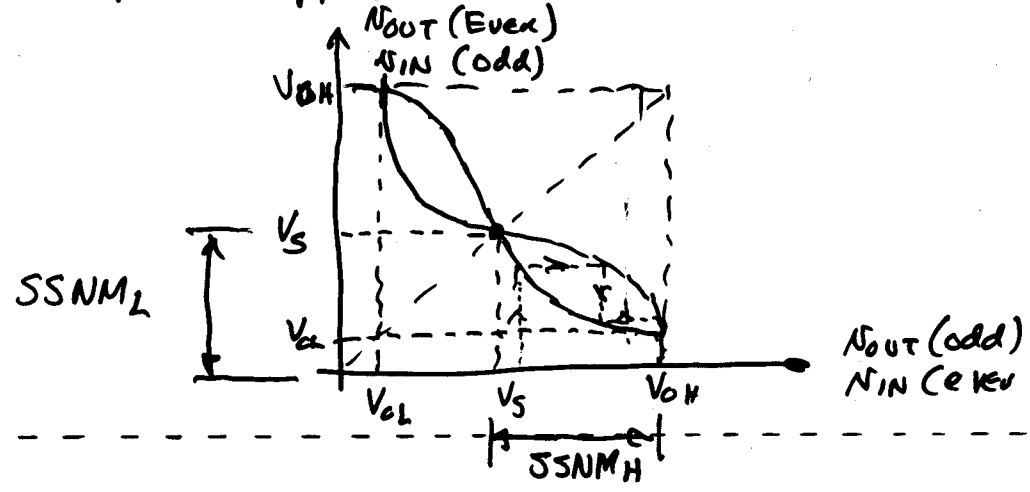
Single-Source Noise Margin

Consider the following





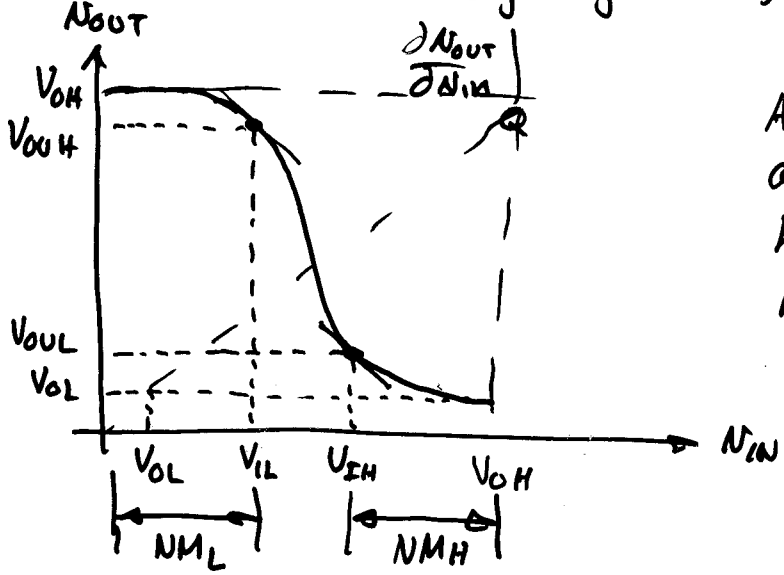
Graphical Approach for General Case –



Multiple-Source Noise Margin

Accounts for noise at all logic nodes.

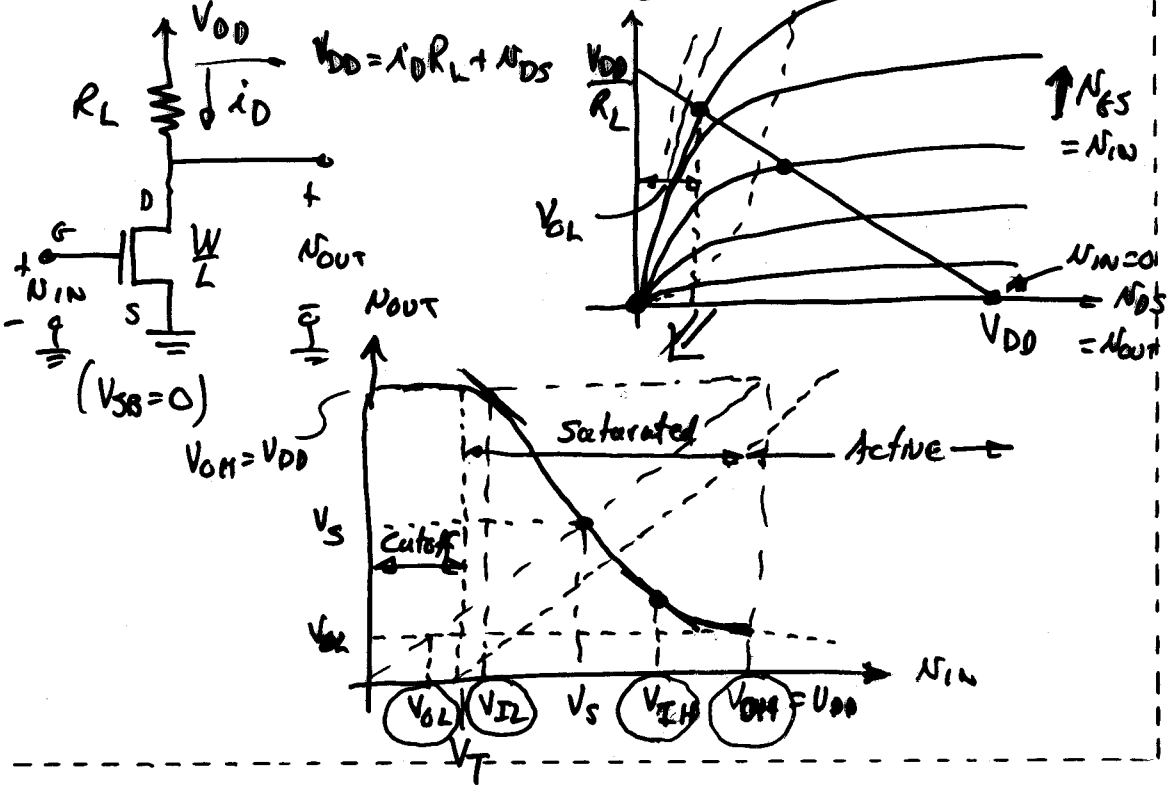
Principle: "If small-signal gain < 1, noise can't grow."



Assumes that all logic gates have a gain magnitude greater than 1 at some point on the voltage transfer characteristics.

RESISTIVE LOAD INVERTER DESIGN

Graphical Perspective



Mathematical Perspective

1.) V_{OH} If $V_{IN} < V_T$, then $V_{OH} = V_{DD}$

2.) $V_{OL} = ?$ Assume that the MOSFET is in the linear region

$\therefore I_{RL} = I_{DS}(\text{linear}) \;\&\; V_{GS} = V_{OH} \;\&\; V_{DS} = V_{OL}$

$$\frac{V_{DD} - V_{OL}}{R_L} = \frac{1}{2}\frac{W_n}{L_n}\left(\frac{\mu_0 C_{ox}}{1 + \frac{V_{OL}}{E_{CLN}}}\right)\left[2(V_{OH} - V_t)V_{OL} - V_{OL}^2\right]$$

$$V_{OL} \simeq \frac{V_{DD}}{1 + k R_L (V_{OD} - V_T)}$$