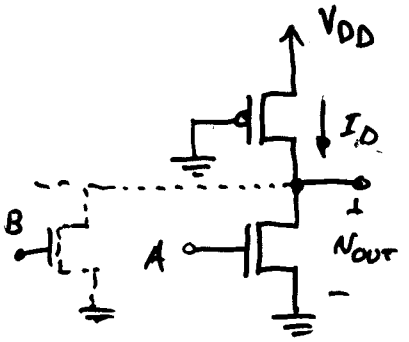
Susanta Sengupta will be lecturing on 2/16 → 2/20
Exam I will be given back on Friday

Pseudo-NMOS Inverters



$V_{OH} = V_{DD}$

$V_{OL} = ?$ → $I_{Dp}(sat) = I_{Dn}(lin)$

$$\frac{W_p \mu_{sat} C_{ox} (V_{DD} - |V_{TP}|)^2}{(V_{DD} - |V_{TP}|) + E_{crLp}} = I_{Dp}(sat) =$$

$$\frac{W_n}{L_n}\left(\frac{\mu_e C_{ox}}{1 + \frac{V_{OL}}{E_{crLn}}}\right)\left[(V_{DD} - V_{TN})(V_{OL}) - \frac{V_{OL}^2}{2}\right]$$

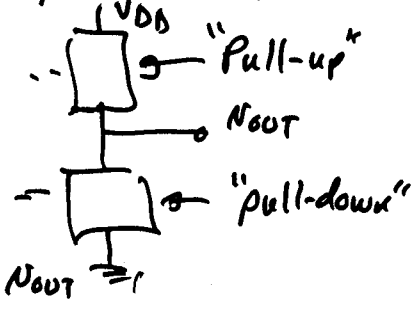
Assume $V_{OL} \simeq 0$

$$\therefore \quad I_{Dp}(sat) \cong \underbrace{\mu_e C_{ox} \frac{W_n}{L_n}}_{k_n} (V_{DD} - V_{TN}) V_{OL} \quad \leftarrow \quad V_{OL} = \frac{I_{Dp}(sat)}{k_n (V_{DD} - V_{TN})}$$

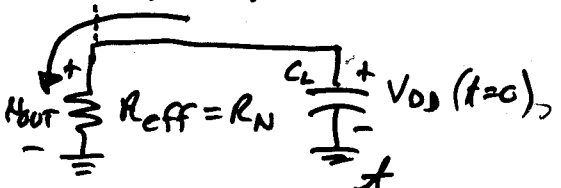
Probably pick V_{OL} → k_n → $\frac{W_n}{L_n}$

Sizing Inverters

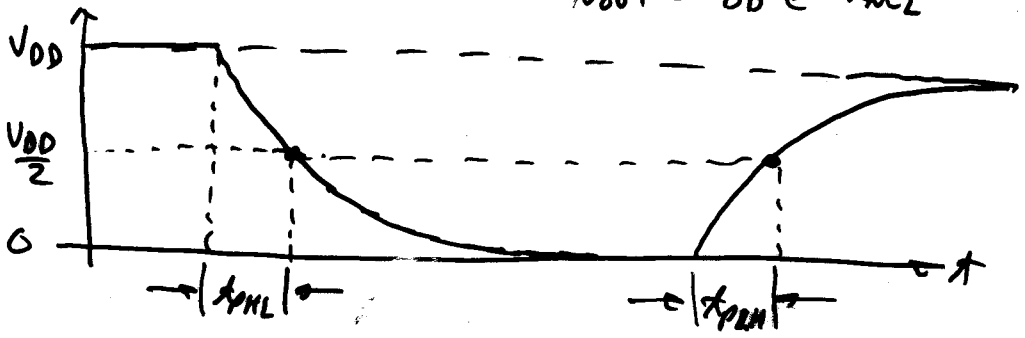
Speed or t_{pHL} and t_{pLH} are focus.



Pull down:



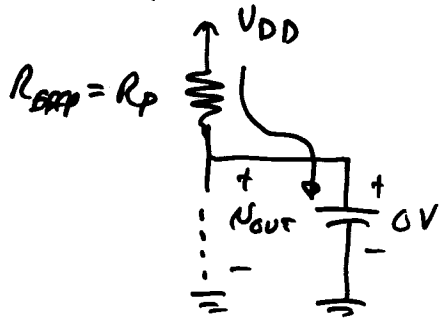
$$N_{OUT} = V_{DD}\, e^{-\frac{t}{R_N C_L}}$$



$$V_{OUT}(t_{PHL}) = 0.5\,V_{DD} = e^{-\frac{t_{PHL}}{R_N C_L}} \rightarrow t_{PHL} = 0.69\,R_N C_L$$

$$t_{PHL} = 0.69\,R_{eff}\,C_L$$

Pull up -



$$V_{OUT}(t) = V_{DD}\left[1 - e^{-t/R_p C_L}\right]$$

$$t_{PLH} = 0.69\,R_p C_L \approx 0.7\,R_p C_L$$

t_{PHL} or t_{PLH} → R_{eff} → $\frac{W}{L}$ "Sizing"

Ex. 4.9 - Sizing of a CMOS & Pseudo-NMOS Inverter

CMOS

Speed is generally the highest priority.

$t = 0.7\,R_{eff}\,C_L = 0.7\,R_{eff}\,50fF = 50ps$ ← Choose 50ps

NMOS:

$$R_{eff} = \frac{50ps}{50fF\,(0.7)} = 1.4k\Omega$$

(C_L = 50fF)

"Constant" for a technology

Know that $R_N = R_{eff} = R_{eqn} \times \frac{L_n}{W_n} = 12.5k\Omega \times \frac{L_n}{W_n}$

$\therefore \frac{L_n}{W_n} = \frac{1}{8.75}$ → $\frac{W_n}{L_n} = 8.75$

PMOS:

$1.4k\Omega = R_p = R_{eqp} \times \frac{L_p}{W_p} = 30k\Omega\,\frac{L_p}{W_p}$ → $\frac{W_p}{L_p} = 21$

If $L_p = L_n = L = 0.1\mu m$, then $W_n = 0.875\mu m$ & $W_p = 2.1\mu m$

Pseudo-NMOS

In this case $V_{OL} = 0.065V$ will be our priority.

$$\frac{W_p N_{sat} C_{ox} (V_{DD} - |V_{Tp}|)^2}{(V_{DD} - |V_{Tp}|) + E_{cp} L_p} = \frac{W_n}{L_n} \frac{\mu_n C_{ox}}{\left(1 + \frac{V_{OL}}{E_{cn} L_n}\right)} \left[(V_{DD} - V_{TN}) V_{OL} - \frac{V_{OL}^2}{2} \right]$$

(V_{DD})

$$\frac{W_p (2\times10^6)(1.6\times10^{-6})(1.2 - 0.4)^2}{(1.2 - 0.4) + 2.4} = \frac{W_n}{L_n} \frac{(270)(1.6\times10^{-6})}{1 + \frac{0.065}{0.6}} \left[(1.2 - 0.4)(0.065) + \frac{0.065^2}{2} \right]$$

Assume the same as the CMOS

$\frac{W_n}{L_n} = 8.75$

$2.56 W_p = 170\times10^{-6} \rightarrow W_p = 0.66\mu m$ $(L_p = 0.1\mu m)$

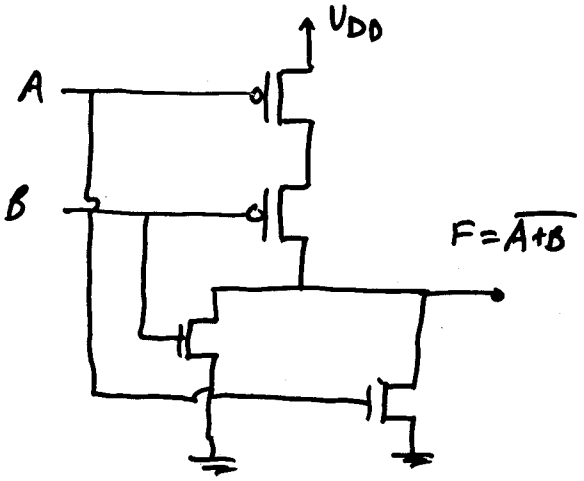
Check t_{PLH}:

$R_{eqp} \times \frac{0.1}{0.66} = 4.54k\Omega \rightarrow t_{PLH} = (4.54k\Omega)(50fF)$ ($R_{eqp} = 30K$)

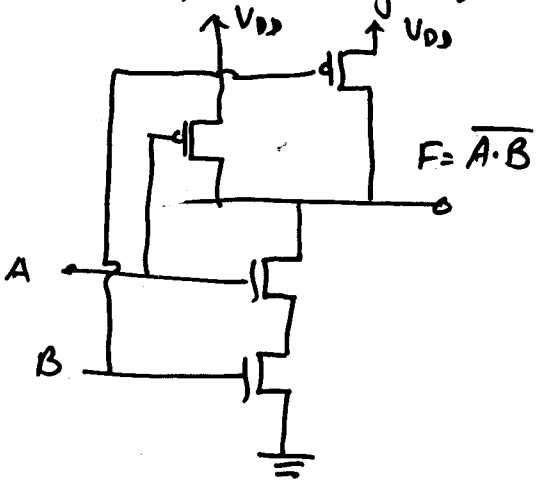
$= 227ps$

CHAPTER 5 – CMOS GATE CIRCUITS

2-input NOR gate:



2-input NAND gate:

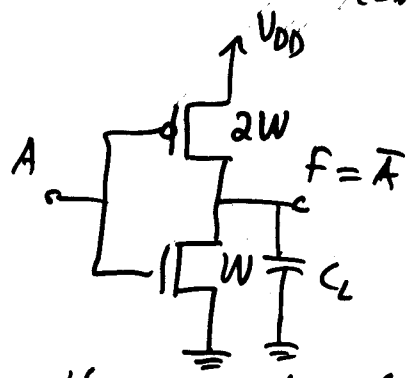


How do you size these transistors?

Basic Gate Sizing

$k = \mu C_{ox} \frac{W}{L}$

Strategy: All sizing will be based on the device sizes shown in the CMOS inverter.



L's are identical ($L_p = L_n$)

Sizing CMOS Gates from a Worst Case Perspective

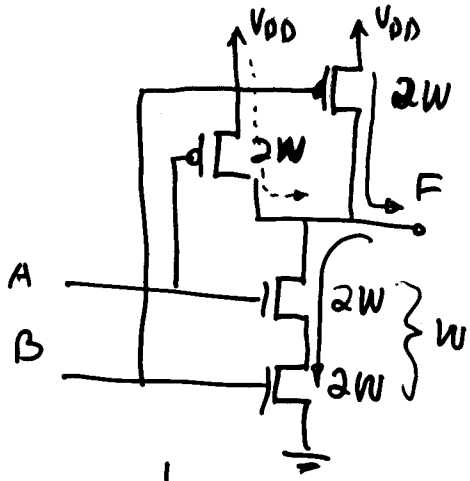
Remember that the effective resistance of a MOSFET can be stated as:

V_{GS} or $|V_{SG}| = V_{DD} \rightarrow R_{MOS} = 0$

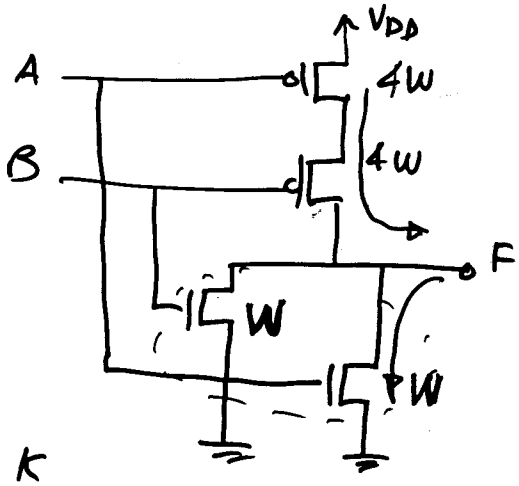
V_{GS} or $|V_{SG}| = 0 \rightarrow R_{MOS} = \infty$

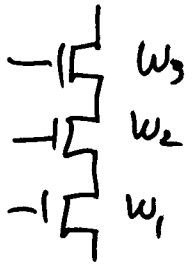
In between these values we use R_{effn} & R_{effp}

2-input NAND:



2-input NOR:





$$R_{MOS} = \frac{k}{W}$$

$$R_{eff} = R_1 + R_2 + R_3 = \frac{k}{W_1} + \frac{k}{W_2} + \frac{k}{W_3} = \frac{k}{W_{eff}}$$

$$W_{eff} = \frac{1}{\frac{1}{W_1} + \frac{1}{W_2} + \frac{1}{W_3}}$$