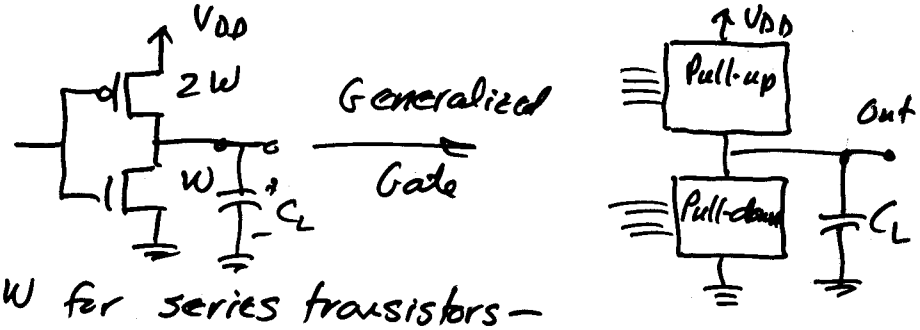
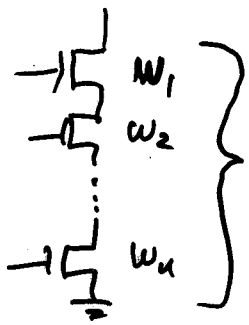
Next week (2/16 – 2/20) Susanta Sengupta will be lecturing in ECE 4420. Tues. 3-4:30 pm office hours will be held.

Sizing of CMOS Gates –

Principle: Make the gate sized such that under worst case conditions it emulates the "std." CMOS inverter.



Effective W for series transistors –

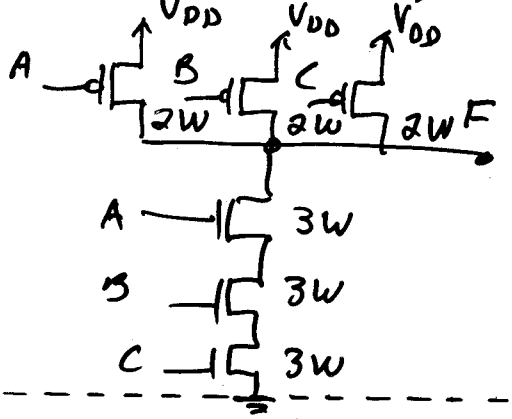


$$W_{eff} = \frac{1}{\frac{1}{W_1} + \frac{1}{W_2} + \cdots + \frac{1}{W_n}}$$

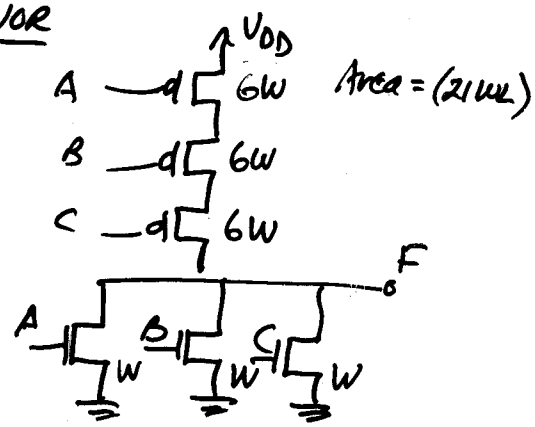
Example 5.1

Determine the device sizes for a 3-input NAND and NOR gates in conventional CMOS.

NAND (Area = 15WL)

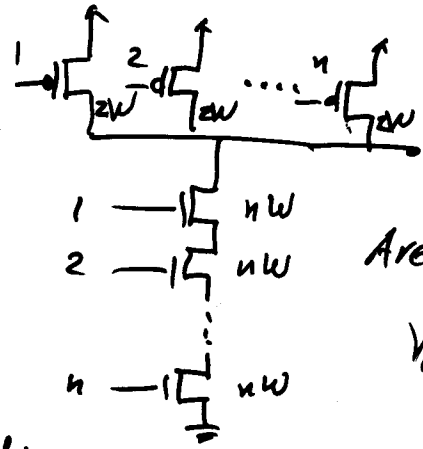


NOR



Fan-In and Fan-Out

Problem? Too many inputs cause too much area.

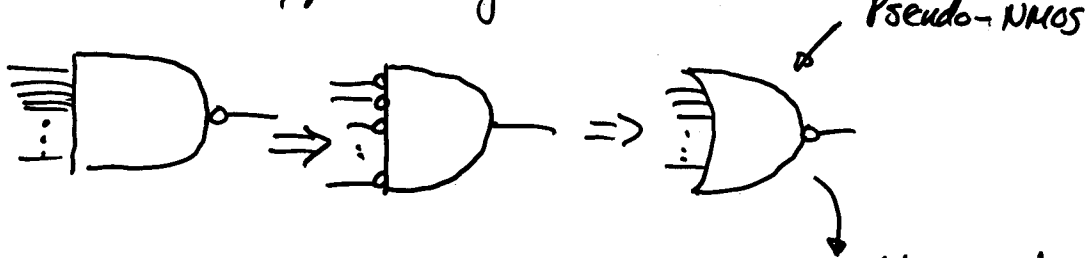


$Area = n^2 WL + nWL \times 2$

V_{OL} starts to grow

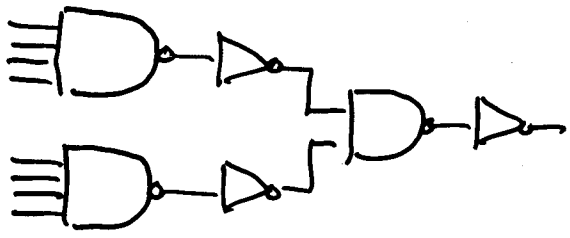
Solutions —

1.) Switch the type of logic

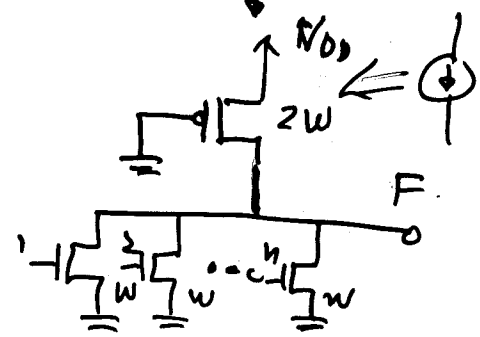


2.) Do the logic in stages

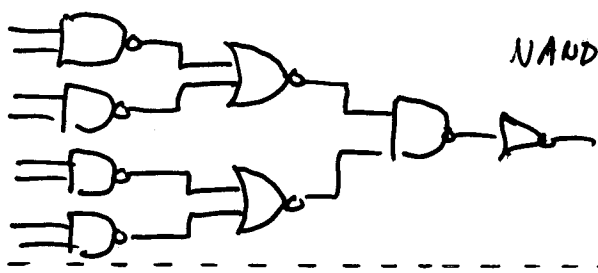
8-input NAND



NAND4 - INV - NAND2 - INV



Tradeoff: Speed vs. area



NAND2 - NOR2 - NAND2 - INV

Fan-Out:

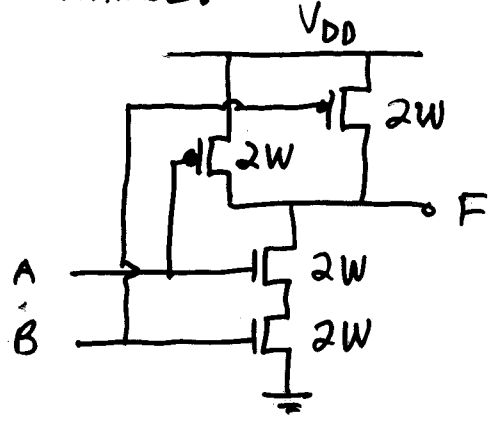
$$\text{Fan Out} = FO = \frac{C_{out}}{C_{gate}} = \text{no. of identical gates driven by the gate under examination.}$$

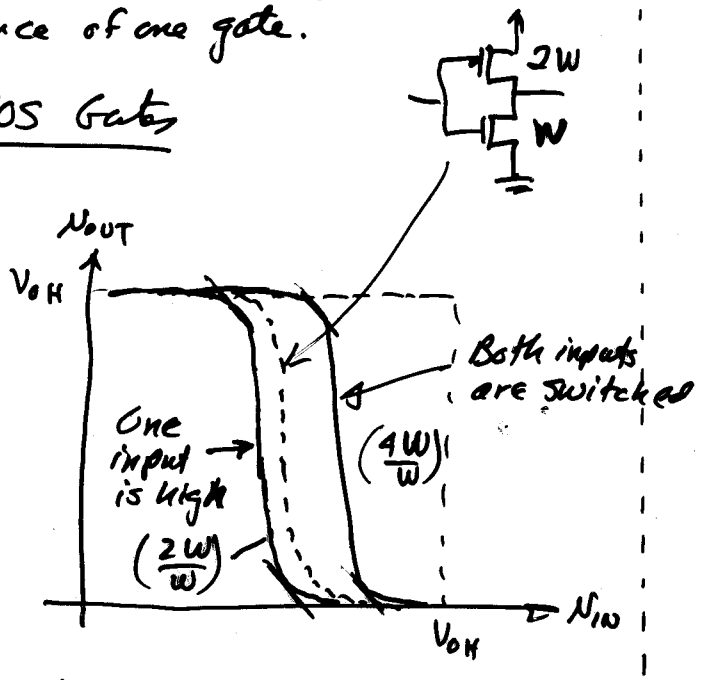
C_{out} = total capacitance driven by the gate

C_{gate} = input capacitance of one gate.

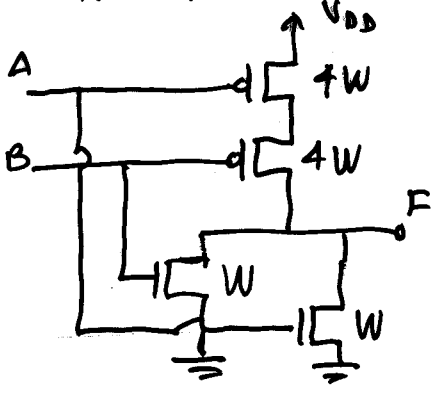
Voltage Transfer of CMOS Gates

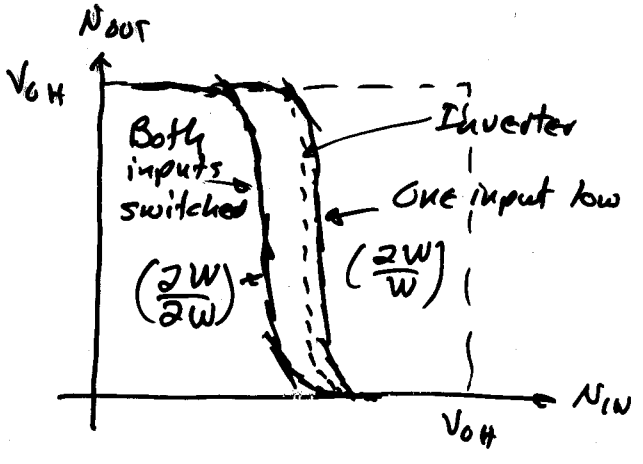
NAND2:





NOR2:



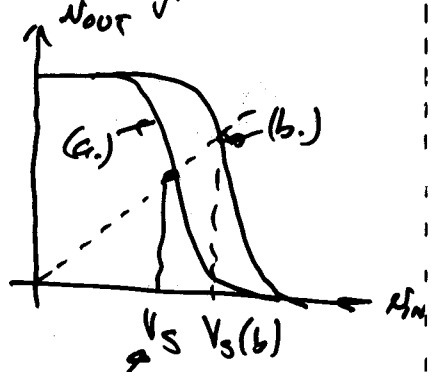


Example 5.2

Compute the value of V_S for a NAND2. a.) One input is at V_{DD} and the other is switched from 0 to V_{DD}. b.) Both inputs are tied together. Assume 0.18 μm technology and $W = 0.4$ μm

a.) $X = \sqrt{\dfrac{\frac{W_n}{\mu_n C_{ox} L_n}}{\frac{W_p}{\mu_p C_{ox} L_p}}} = 2$

$W_n = 400$ nm
$W_p = 400$ nm
$L = 200$ nm



$$V_S = \frac{V_{DD} - |V_{TP}| + X V_{TN}}{1 + X} = \frac{1.8 - 0.5 + 2(0.5)}{1+2} = 0.77\,V$$

b.) With both inputs tied together → $W_p = 800$ nm and $W_n = 200$ nm

$X = 1 \rightarrow V_S = 0.9\,V$