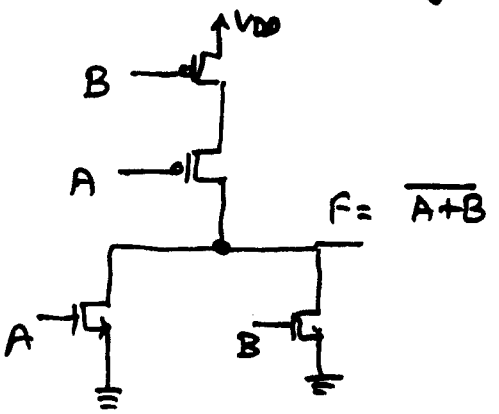
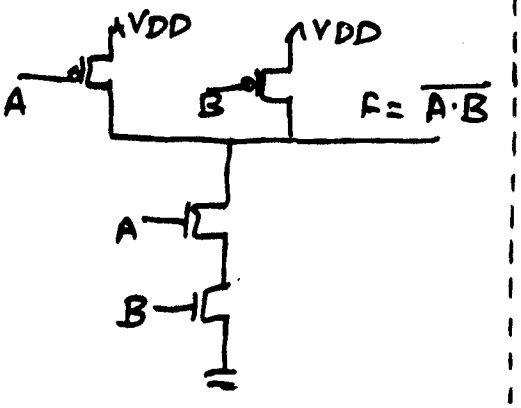
CMOS Gate Circuits

2-input NOR gate

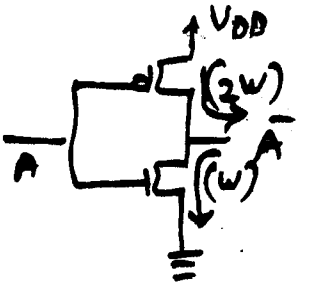


2-input NAND gate



Basic gate sizing

All sizing will be based on the device sizes of the CMOS inverter

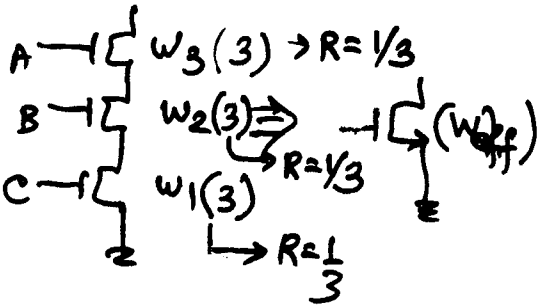


Worst-case gate sizing (from speed point of view)

Assume that when V_{GS} or $|V_{SG}| = V_{DD}$, $R_{MOS} = 0$

and when V_{GS} or $|V_{SG}| = 0$, $R_{MOS} = \infty$

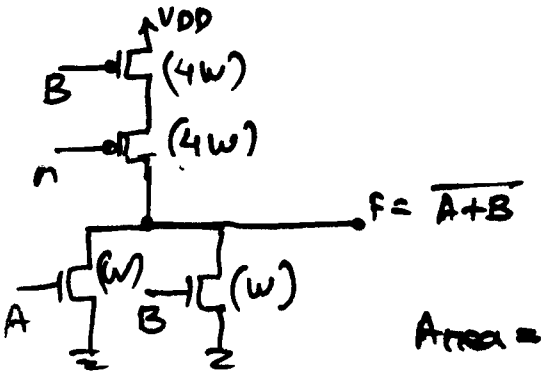
Effective W for series transistors

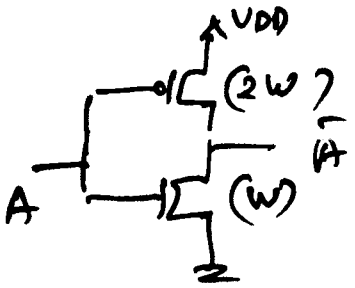


$$R_{MOS} = \frac{K}{W}$$

$$W_{eff} = \frac{1}{\left(\frac{1}{W_1} + \frac{1}{W_2} + \frac{1}{W_3}\right)}$$

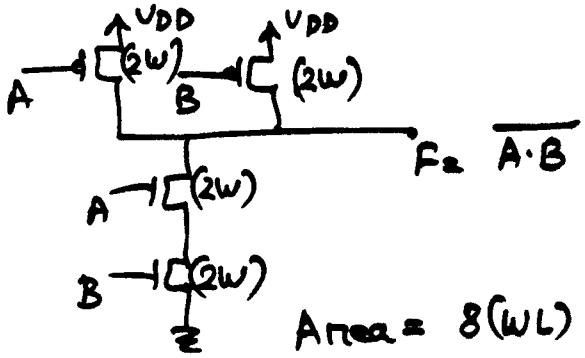
2-input NOR

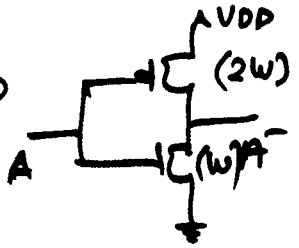




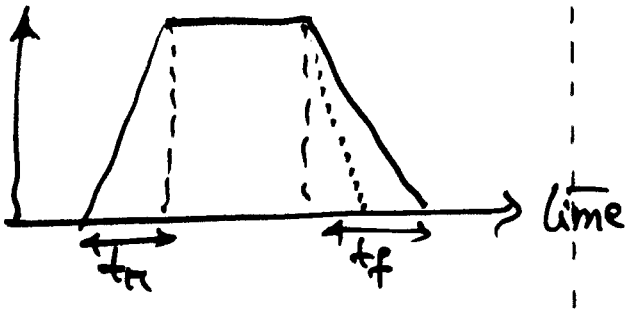
Area = 10(WL)

2-input NAND

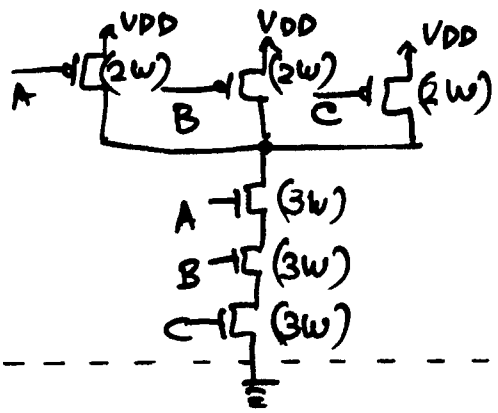




Area = 8(WL)

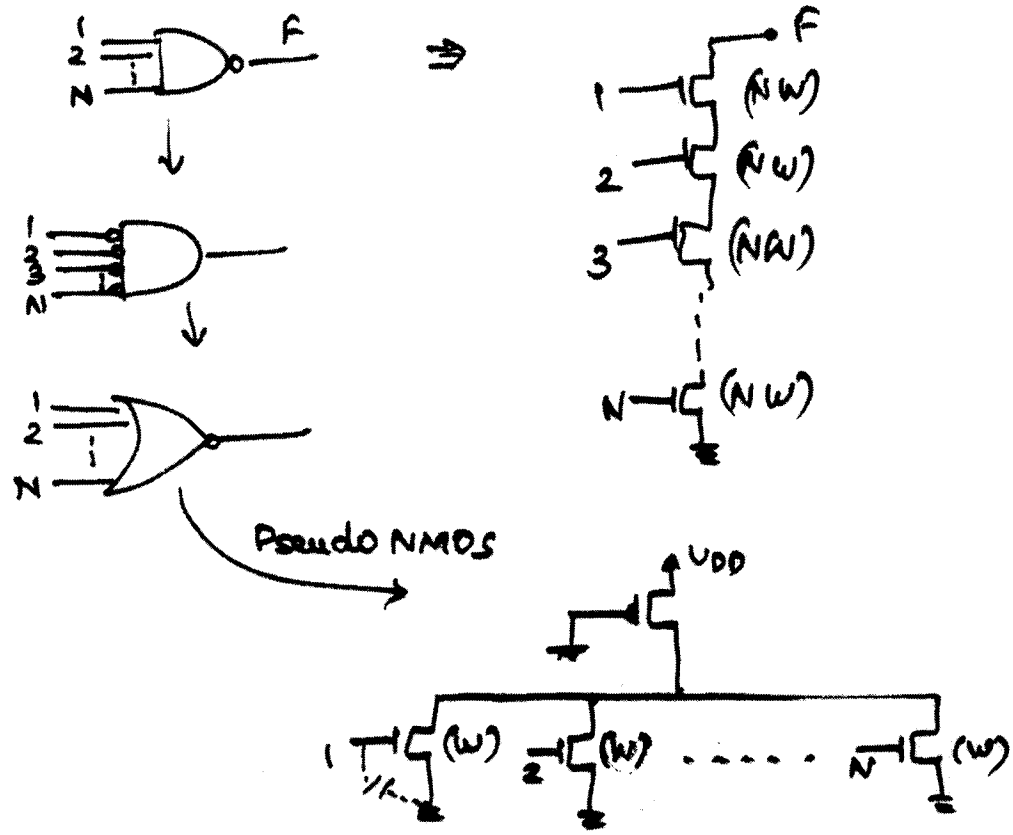


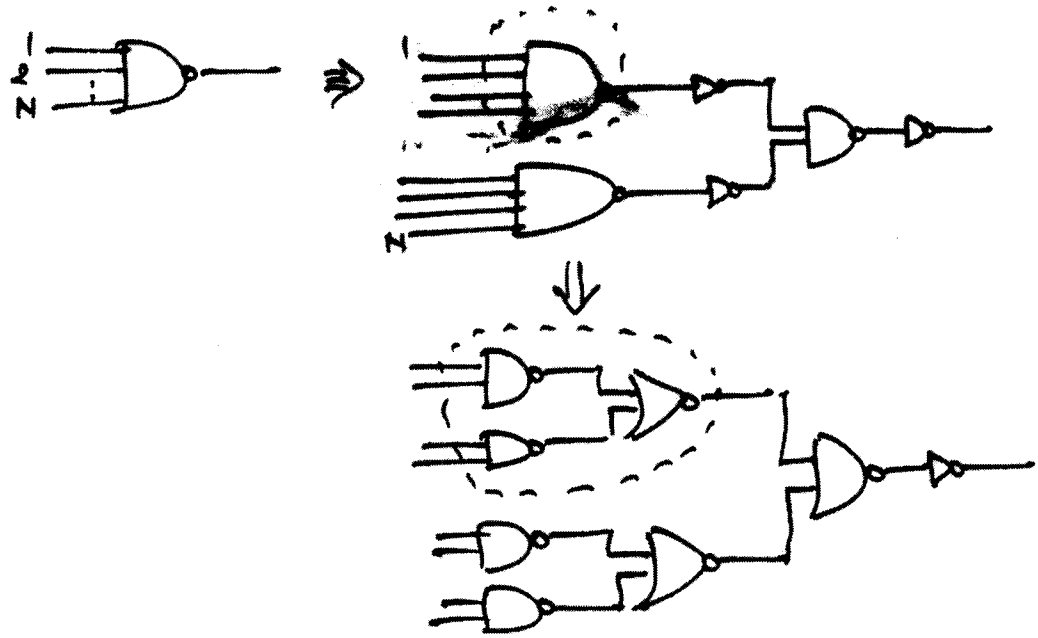
3-input NAND gate



Fan-in and fan-out

Fan-in :-

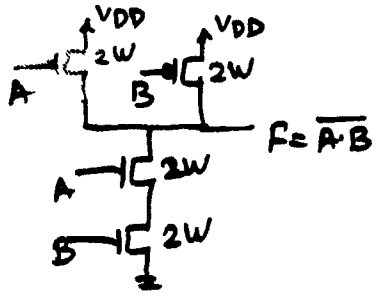
① 

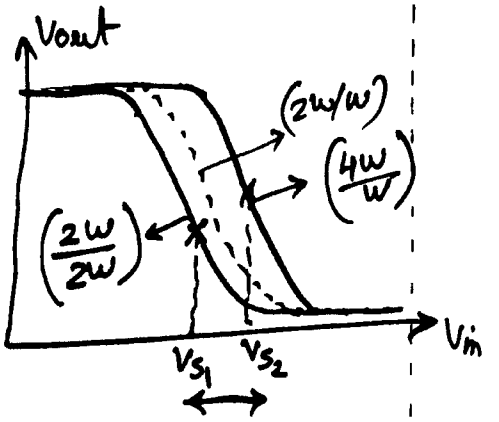
② 

Fan out = $\frac{C_{out}}{C_{gate}}$ = $\frac{\text{Total capacitance driven by the gate}}{\text{input capacitance of the gate}}$

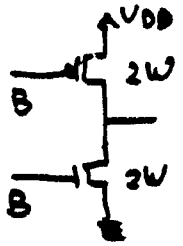
VTC

NAND2

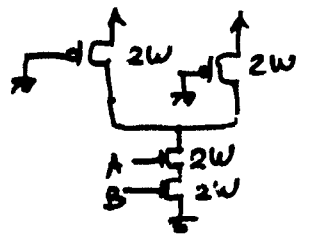




① A = 1
B = 0 → 1 →



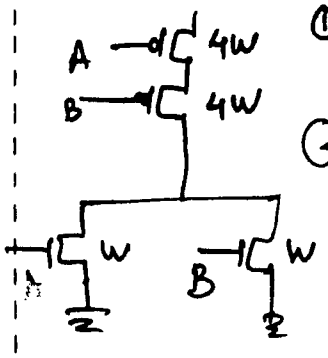
② A = 0 → 1
B = 0 → 1



Ex. 5.2

$V_{S_1} = 0.77V$, $V_{S_2} = 0.9V$

NOR2



① A = 0
B = 0 → 1

② A = 0 → 1
B = 0 → 1