CMOS Gate Circuits

2-input NOR gate

A
\[ F = \overline{A+B} \]

2-input NAND gate

A
\[ F = \overline{A \cdot B} \]

Basic gate sizing

All sizing will be based on the device sizes of the CMOS inverter.

Worst-case gate sizing (from speed point of view)

Assume that when \( V_{ds} = 0 \) or \( |V_{gs}| = V_{dd} \), \( R_{mos} = 0 \) and when \( V_{gs} = 0 \) or \( |V_{ds}| = 0 \), \( R_{mos} = \infty \).

Effective \( W \) for series transistors

\[ R_{mos} = \frac{K}{W} \]

\[ W_{eff} = \frac{1}{\left(\frac{1}{w_1} + \frac{1}{w_2} + \frac{1}{w_3}\right)} \]
2-input NOR

\[ A \overline{W} \quad (4W) \]

\[ B \overline{W} \quad (4W) \]

\[ F = \overline{A + B} \]

\[ \text{Area} = 10(\mu\text{L}) \]

2-input NAND

\[ A \overline{W} \quad (2W) \]

\[ B \overline{W} \quad (2W) \]

\[ F = \overline{A \cdot B} \]

\[ \text{Area} = 8(\mu\text{L}) \]

3-input NAND gate

\[ A \overline{W} \quad (2W) \]

\[ B \overline{W} \quad (2W) \]

\[ C \overline{W} \quad (2W) \]

\[ F = \overline{A \cdot B \cdot C} \]

\[ \text{Area} = 15(\mu\text{L}) \]
Fan-in and Fan-out

Fan-in:

1. \[ F \]

2. \[ UDD \]

Pseudo NMOS

\[ (W) \]

\[ (NW) \]

\[ (NW) \]

\[ (NW) \]

\[ (NW) \]

\[ (NW) \]
Fan out = \frac{\text{Cout}}{\text{Cgate}} = \frac{\text{Total capacitance driven by the gate}}{\text{Input capacitance of the gate}}

\[ \text{VTC} \]

\[ \text{NAND2} \]

1. \( A = 1 \) 
   \( B = 0 \to L \) 

2. \( A = 0 \to 1 \) 
   \( B = 0 \to 1 \)

Ex. 5.2

\( V_{S1} = 0.77V, \quad V_{S2} = 0.9V \)

\[ \text{NOR2} \]

1. \( A = 0 \) 
   \( B = 0 \to L \)

2. \( A = 0 \to 1 \) 
   \( B = 0 \to 1 \)