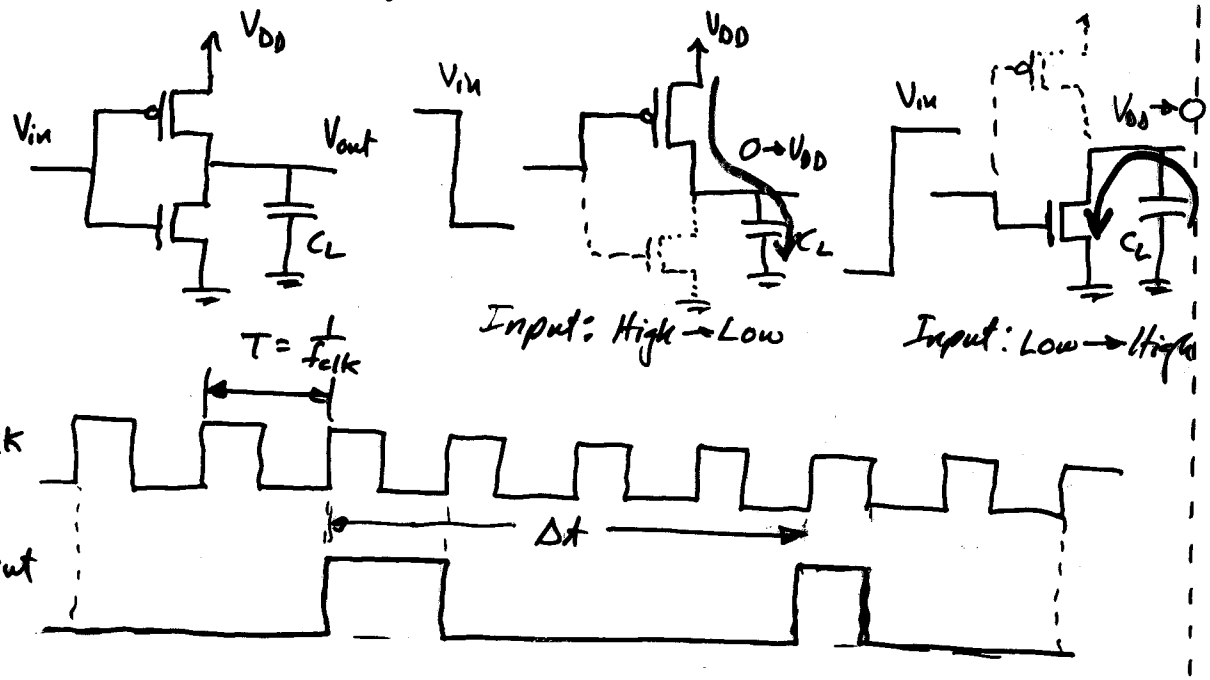
Power Dissipation in CMOS Gates (Sec. 5.5)

Types of Power

Dynamic – capacitive switching, short-circuit, & glitches
Static – leakage current and dc standby power

Dynamic (Switching) Power



$$I_D(aver.) = C\frac{dv}{dt} = C_L \frac{\Delta V_{swing}}{\Delta t} = \frac{C_L V_{DD}}{\Delta t} = C_L V_{DD} f_{aver.}$$

$$f_{aver} = \frac{1}{\Delta t}$$

$$P_{switching} = I_D(aver) V_{DD} = C_L V_{DD}^2 f_{aver.} = \alpha_{0\to1} C_L V_{DD}^2 f_{CLK}$$

where $\alpha_{0\to1} = \frac{f_{aver.}}{f_{CLK}} = \frac{(\text{No. of toggles}/2)}{\text{No. of clock cycle}} = \frac{4/2}{8} = \frac{1}{4}$

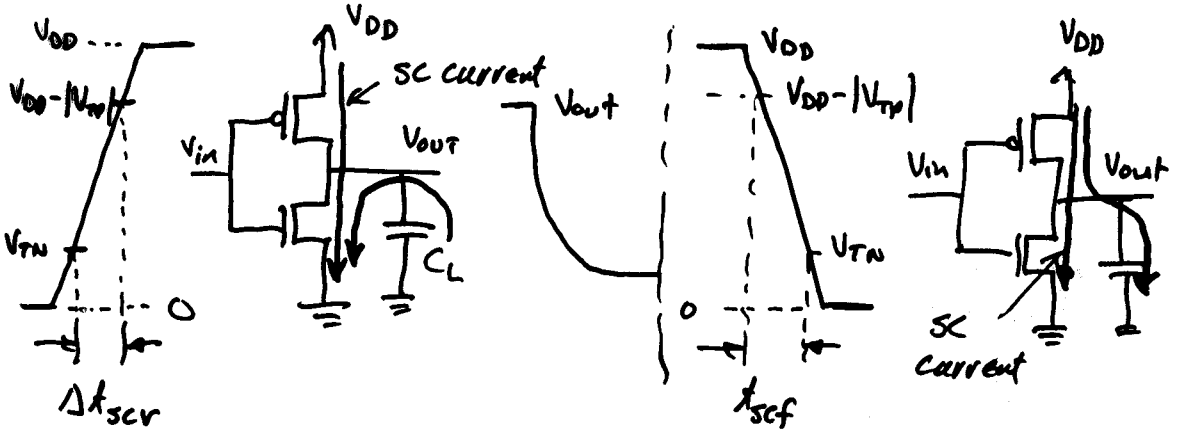
Example

Compute the switching power for an inverter with $C_L = 50fF$ and $f_{aver.} = 250MHz$. Let $V_{DD} = 1.8V$

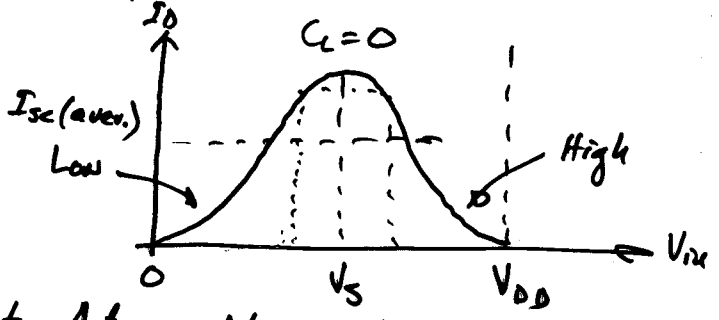
$$P_{switching} = CV^2 f_{aver} = (50fF)(1.8V)^2(250MHz) = 40.5\mu W$$

(SPICE gives 46.3 μW)

Dynamic Short-Circuit power —



Another way to visualize the short-circuit is,



Let $\Delta t_{sc} = \Delta t_{scr} + \Delta t_{scf}$

$P_{sc} = I_{sc} V_{DD}$ $I_{sc} = ?$ $I_{sc} = I_{sc(aver)} \frac{\Delta t_{sc}}{T}$

$P_{sc} = \frac{\Delta t_{sc}}{T} I_{sc(aver)} V_{DD} = \Delta t_{sc} I_{sc(aver)} V_{DD} f_{CLK}$

$I_{sc(aver)} = ?$

Let $I_{sc(aver.)} = C\frac{dv}{dt} = C_{sc}\frac{V_{DD}}{\Delta t_{sc}}$

$\therefore P_{sc} = C_{sc} V_{DD}^2 f_{clk} = \alpha_{sc} C_L V_{DD}^2 f_{CLK}$

$\alpha_{sc} = \frac{C_{sc}}{C_L}$ = switching activity factor

$P_{Dynamic} = P_{switching} + P_{sc} + P_{static} = \alpha_{0\to1} C_L V_{DD}^2 f_{CLK} + \alpha_{sc} C_L V_{DD}^2 f_{CLK}$

$= (\alpha_{0\to1} + \alpha_{sc}) C_L V_{DD}^2 f_{CLK} = \alpha C_L V_{DD}^2 f_{CLK}$

STATIC POWER –

Leakage + static power

Sources of leakage –

1.) Subthreshold: $I_{sub} = I_s \exp\left[\frac{q(V_{GS} - V_T - V_{offset})}{nkT}\right]\left[1 - \exp\left(\frac{-qV_{DS}}{kT}\right)\right]$

2.) PN Junction: $I_{pn} = I_o\left[\exp\left(\frac{qV_{SB}}{kT}\right) - 1\right]$, $I_o = A J_s$

$\therefore P_{static} = (I_{sub} + I_{pn}) V_{DD} = I_{Leak} V_{DD}$

Pseudo-NMOS

This logic has static current flow, I_{DC}, when $V_{OUT} = V_{OL}$

$P_{DC} = V_{DD} I_{DC}$

Complete Static Power

CMOS: $P = \alpha C V_{DD}^2 f_{clk} + I_{leak} V_{DD}$

Pseudo-NMOS: $P = \alpha C V_{DD}^2 f_{clk} + I_{leak} V_{DD} + I_{DC} V_{DD}$

Power vs. Delay Tradeoffs

Power-delay product = PDP = $P_{aver.} \times t_p$

$= (C V_{DD}^2 f_{clk})\left(\frac{1}{2 f_{clk}}\right) = \frac{C V_{DD}^2}{2}$ (Energy)

Great metric, but it is difficult to compare designs with.

$\therefore$ We use an energy-delay product EDP

$EDP = PDP \times t_p$

$t_p = \frac{C\Delta V}{I} = \frac{C\Delta V}{I_{sat}}$

$I_{sat.} = K_2(V_{GS} - V_T)$ when V_{DD} becomes small

$t_p = \frac{C V_{DD}}{K_2(V_{DD} - V_T)}$

$\therefore \boxed{EDP = \frac{C V_{DD}^2}{2} \frac{C V_{DD}}{K_2(V_{DD} - V_T)} = \frac{C^2 V_{DD}^3}{2 K_2 (V_{DD} - V_T)}}$

$V_{DD}(opt.) = 1.5 V_T$