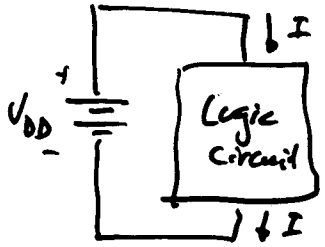
(Check on date of Exam #3)



$J_{DS} = 550 mA/mm$!?

CHAPTER 6 – HIGH SPEED CMOS LOGIC DESIGN

Introduction

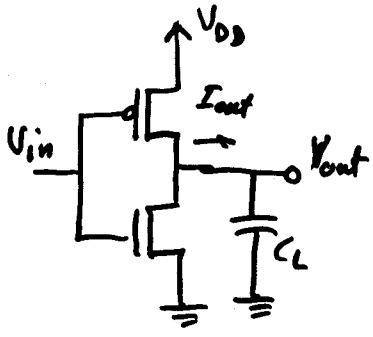
- Goal is to maximize the speed of a logic circuit while minimizing the power and the area.
- Speed is characterized by the propagation delay.

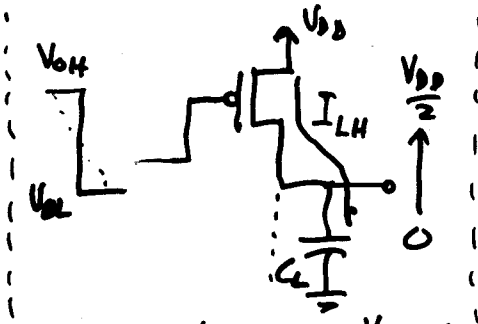
  t_{PHL} is the time to go from V_{DD} to $0.5V_{DD}$.

  t_{PLH} " " " " " " 0 to $0.5V_{DD}$.

$$t_p = \frac{t_{PHL} + t_{PLH}}{2}$$

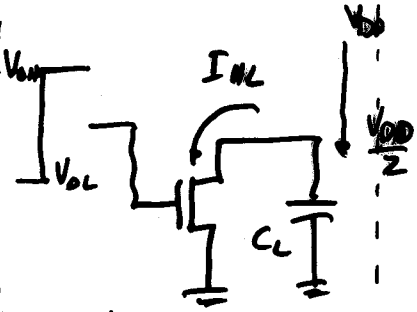
Switching Time Analysis for CMOS gate





$$t_{PLH} = C_L \frac{V_{DD}}{2} \frac{1}{I_{LH}}$$

$I = C \frac{\Delta V}{\Delta T}$



$$t_{PHL} = \frac{C_L V_{DD}}{2 I_{HL}}$$

$$\therefore t_p = \frac{t_{PLH} + t_{PLH}}{2}$$

What is I_{LH} and I_{HL}?

1.) I_{LH} = ? Assume 0.13 μm technology

$V_{DS}(sat.)$ = ? $V_{DS}(sat.) = \frac{(V_{GS}-V_T)E_cL}{(V_{GS}-V_T)+E_cL} = \frac{(1.2-0.4)(2.4)}{(1.2-0.4)+2.4} = 0.6V$

∴ PMOS is ≃ saturated

$I_{LH} = (I_{D,sat})_p \rightarrow t_{PLH} = \frac{C_L V_{DD}}{2(I_{D,sat})_p} = 0.7 R_p C_L$

$\therefore R_p = \frac{V_{DD}/2}{0.7(I_{D,sat})_p} = R_{eqp}$

2.) I_{HL} = ?

$V_{Dsat} = 0.34\,V \rightarrow V_{DS} > V_{DSsat} \Rightarrow$ NMOS is sat.

$t_{PHL} = \frac{C_L V_{DD}}{2(I_{D,sat})_n} = 0.7 R_N C_L \rightarrow R_N = \frac{V_{DD}/2}{0.7(I_{D,sat})_n} = R_{eqn}$

Example 6.1

Using 0.13μm technology, find R_{eqn} & R_{eqp} ($W_n = W_p = 0.1\mu m$)

NMOS:

$I_{Dsat} = \frac{W_n N_{sat} C_{ox}(V_{DD}-V_T)^2}{(V_{DD}-V_T)+E_{CN}L_n} = \frac{(0.1\times10^{-4})(8\times10^{-6})(1.1\times10^{-6})(1.2-0.4)^2}{(1.2-0.4)+2.4}$

$= 58.5\,\mu A$ (Note: that if $W_N = 1\mu m$, then $I_{DS} = 585\,\mu A$ so that is where $I_{DS} = 550\mu A/\mu m$ came from in P5.11)

$R_{eqn} = R_n = \frac{1.2/2}{0.7(58.5\mu A)}$

$= 14.65\,k\Omega \rightarrow$ **$R_{eqn} = 12.5\,k\Omega/\square$**

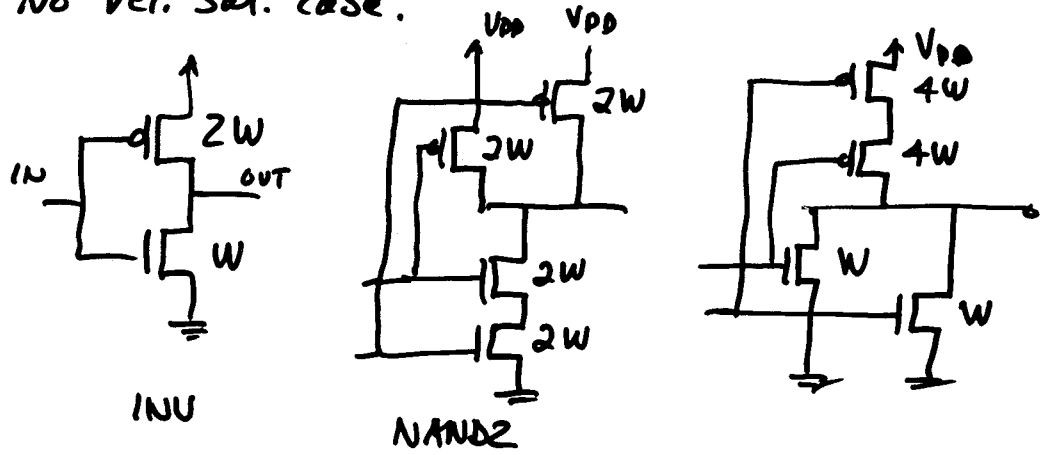
PMOS:

$I_{Dsat} = 26\mu A \rightarrow R_{eqp} = \frac{1.2/2}{0.7(26\mu A)} = 32.97\,k\Omega$

$R_{eqp} = 30\,k\Omega/\square$

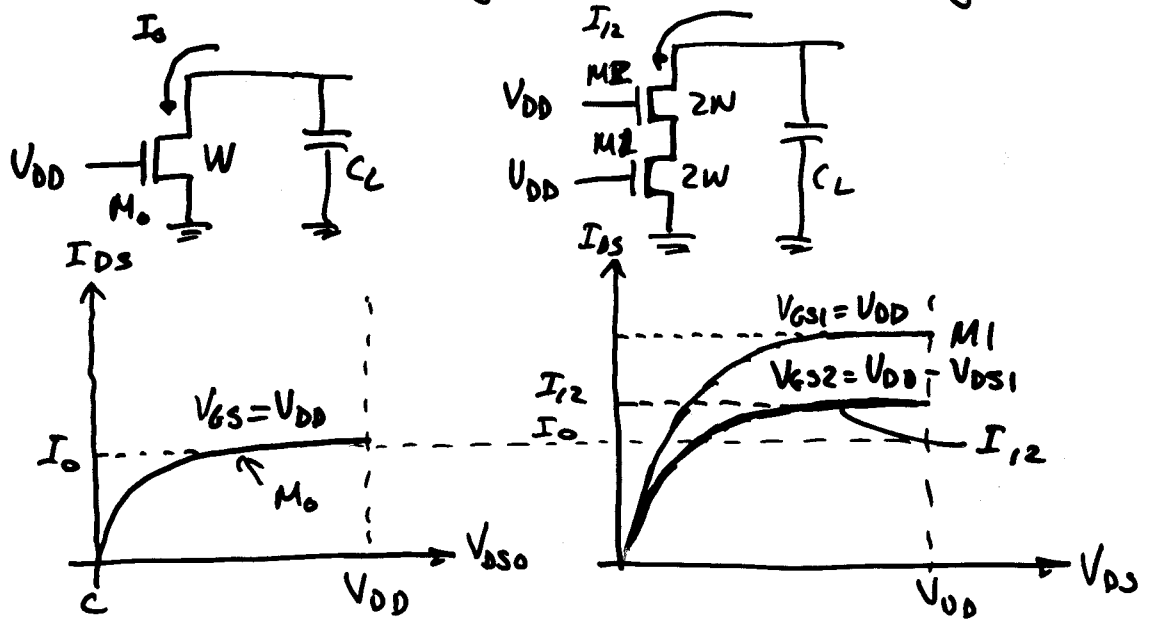
Logic Gate Sizing Including Velocity Sat. Effects

No vel. sat. case:



What is the influence of vel. sat. on this sizing?

Compare the sinking current of the following 2 cases:



$I_{12} \simeq 1.2 I_0$

Comment: If the transistor (M1 & M2) were not vel. saturated, the square law characteristics would force $I_{12} < I_0$