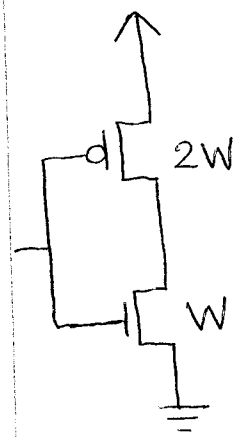
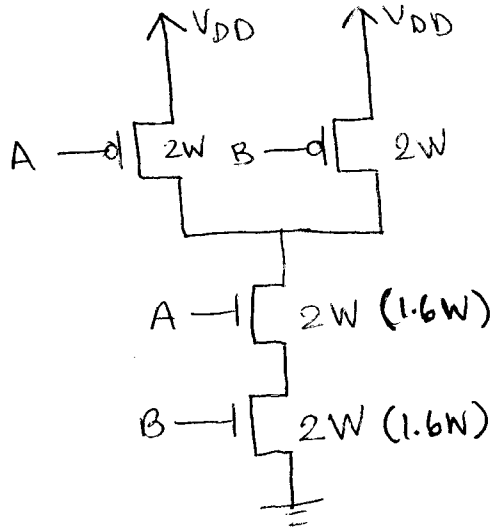
Logic Gate Sizing Including Velocity Sat.

Conclusion: Although velocity saturation changes the gate sizing, we will ignore it.

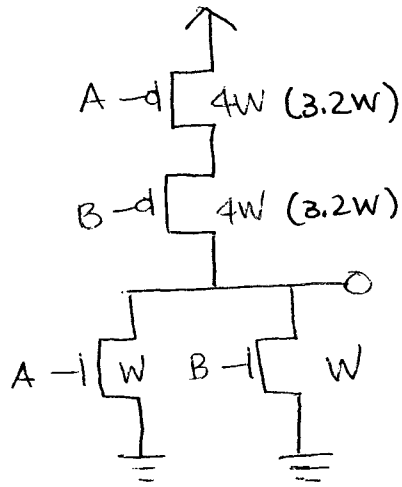
Inverter



NAND2

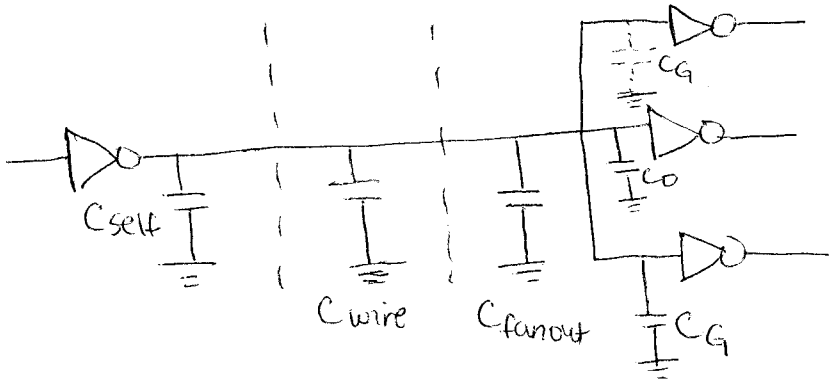


NOR2



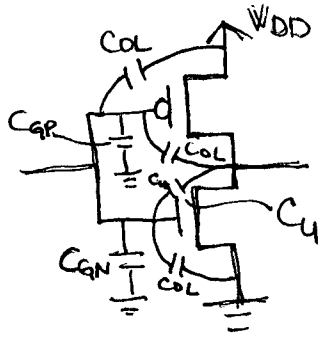
"FO4 Rules"

Load capacitance Calculation



$C_L = C_{self} + C_{wire} + C_{fanout}$

1.) Fanout Capacitance



$$C_{fanout} = \sum_i C_{Gi}$$

$$C_G = C_{GN} + 2C_{OL} + C_{GP} + 2C_{OL}$$

$$C_G = C_{ox} W_N L + 2C_{OL} W_N + C_{ox} W_P L + 2C_{OL} W_P$$

$$= (C_g + 2C_{OL})(W_n + W_p) \qquad C_G = C_g L$$

$C_G = (\overbrace{C_{ox} + 2C_{OL}}^{C_g})(W_p + W_n)$

$C_{ox} + 2C_{OL} = 1.6\,fF/\mu m + 2(0.25\,fF/\mu m) \approx 2\,fF/\mu m$

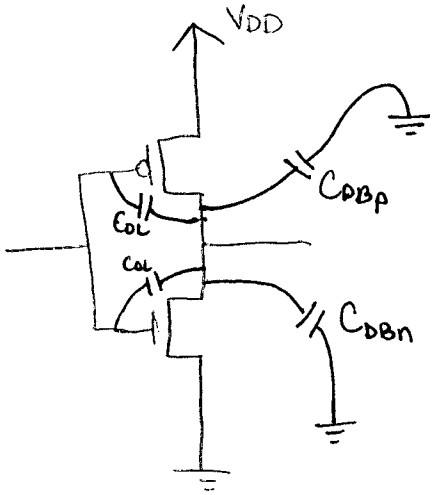
Spice $\rightarrow$ $2.2\,fF/\mu m$

* $\boxed{C_g \approx 2\,fF/\mu m}$ works for both the $0.18\mu m$ and $0.13\mu m$ technology

$C_{fanout} = \sum C_G = \sum_{i=1}^{n} C_{gi}(W_n + W_p)_i$

$= 2\,fF/\mu m\,[(W_{n1} + W_{p1}) + (W_{n2} + W_{p2}) + \ldots + (W_{ni} + W_{pi})]$

2.) Self capacitance



$C_{self} = C_{DBn} + C_{DBp} + 2C_{OL} + 2C_{OL}$

$C_{self} = C_{jn}W_n + C_{jp}W_p + 2C_{OL}(W_n + W_p)$

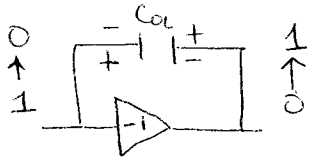
? ? ?

Back to Example 2.12 (NMOS)

$C_j = 0.18\,fF/\mu m \rightarrow 0.22\,fF/\mu m$ including the PMOS

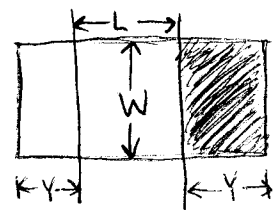
$\Rightarrow 0.5\,fF/\mu m$

$2C_{OL} \Rightarrow$ twice V_{DD} charge



$W = 0.4\,\mu m$ & $L = 0.1\,\mu m$

$Y = 0.3\,\mu m$



The pn capacitance at the gate output $\simeq 0.5fF/\mu m$

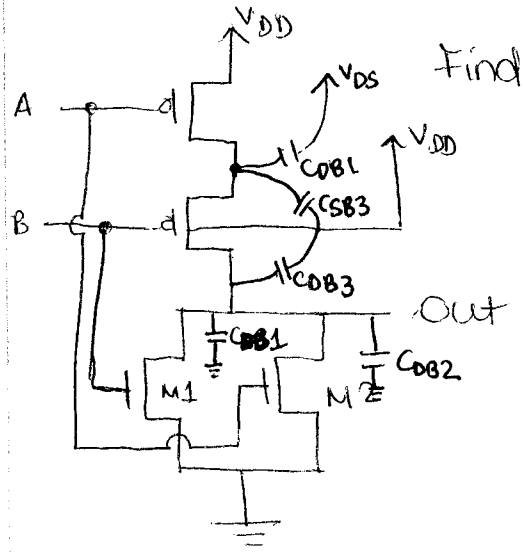
$$C_{self} = (0.5fF/\mu m)(W_n + W_p) + 2C_{OL}(W_n + W_p)$$

C_{OL}: $0.25fF/\mu m$ (from Example 2.13)

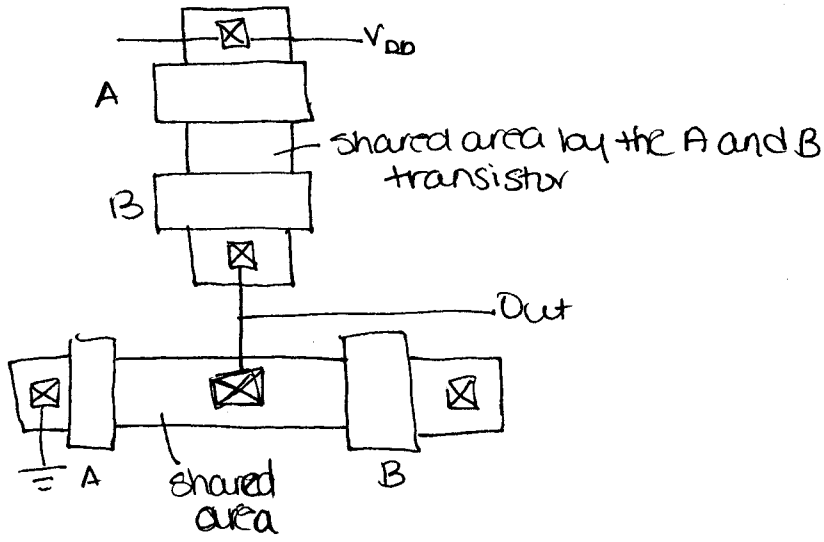
$C_{self} \simeq 1fF/\mu m$ *

SPICE → from low to high at the output
$0.7fF/\mu m$
from high to low : $0.8fF/\mu m$

Capacitance of NOR2



Find Cin and Cout



$$C_{self(pn\ only)} = \underbrace{C_{DB1} + C_{DB2}}_{\text{Shared}} + C_{DB3} + \underbrace{C_{SB3} + C_{DB3}}_{\text{Shared}} \cdots$$