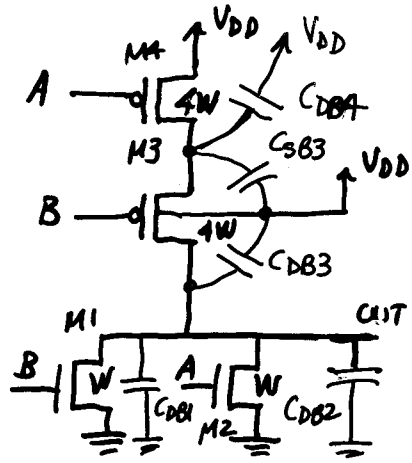
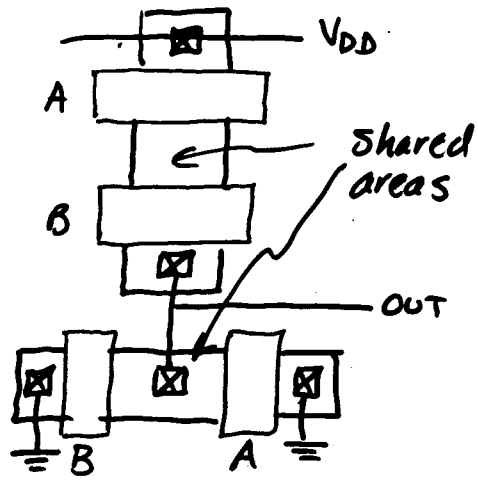
Capacitance of NOR2 (Problem session – Thurs. 3/4 at 7pm)





$$C_{Load} = C_{self} = \underbrace{C_{DB1} + C_{DB2}}_{\text{shared}} + C_{DB3} + \underbrace{C_{SB3} + C_{DB4}}_{\text{shared}}$$

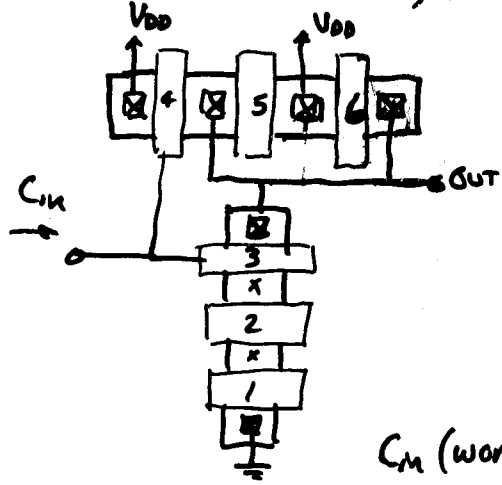
$$C_{Load} = C_{eff}(W_n) + C_{eff}(W_p) + C_{eff}(W_p)$$

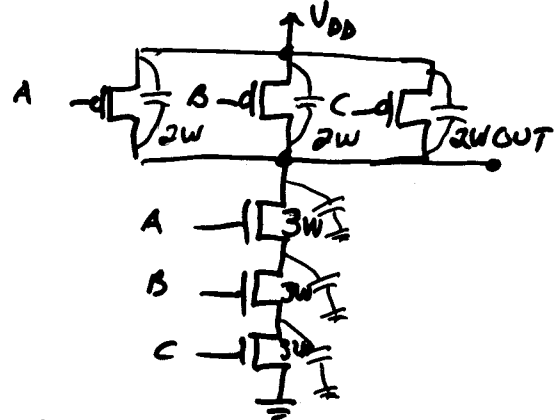
$$= C_{eff}[W_n + 2W_p] = 9W C_{eff} = 9W\,(1fF/\mu m)$$

$$C_{in}\,(\text{worst case}) = C_g(W_n + W_p) = 5W C_g = 5W\,(2\,fF/\mu m)$$

NAND3 Example

Find C_{in} (worst case) and C_{load} if $W = 0.4\mu m$.



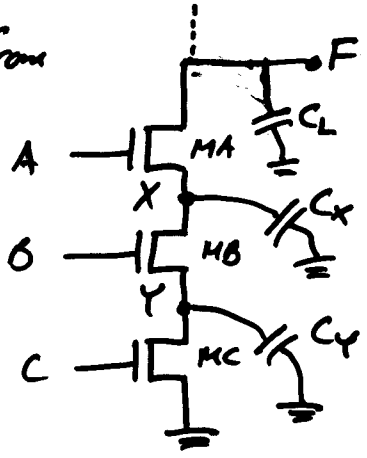


C_{in} (worst case) $= C_g(W_n + W_p) = 5WC_g = 5(0.4)(2) = 4fF$

$C_{load} = C_{self}[2W_p + 3W_n] = (1fF/\mu m)[4W + 9W] = 13(0.4)(1) = 5.2\,fF$

Switching Implications on Gates from a Speed Viewpoint

In a series logic stack, the delay from the input to the output increases the further away a transistor is from the output.



Suppose the following circumstances:

1.) A is late, only C_L needs to be charged

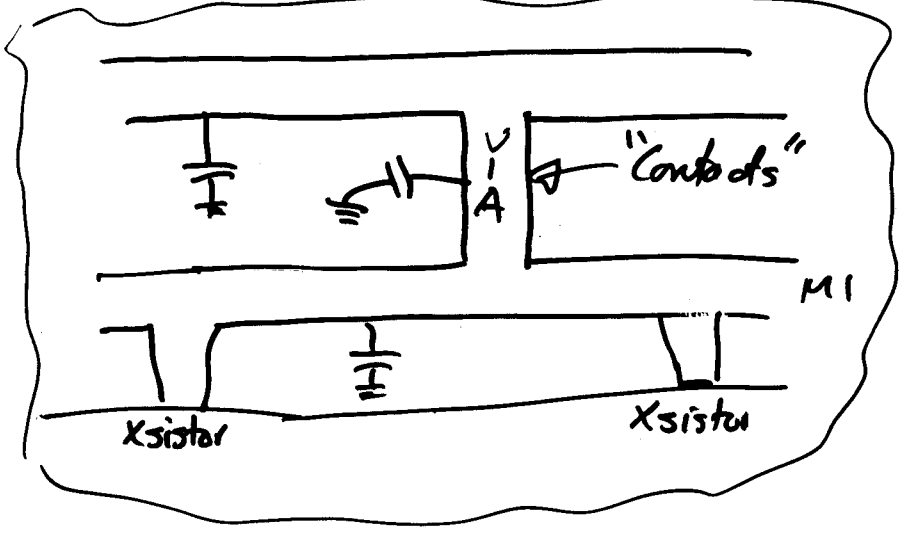
2.) If B is late, both C_X and C_L must be charged.

3.) If C is late, the $C_L + C_X + C_Y$ must be charged.

∴ Move a transistor with a delayed input closest to the output.

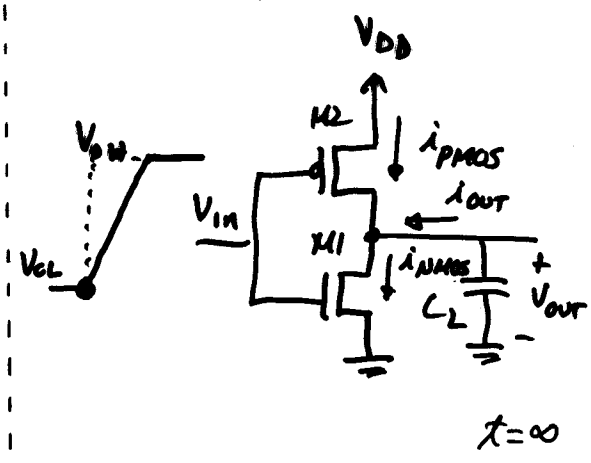
Wiring Capacitance

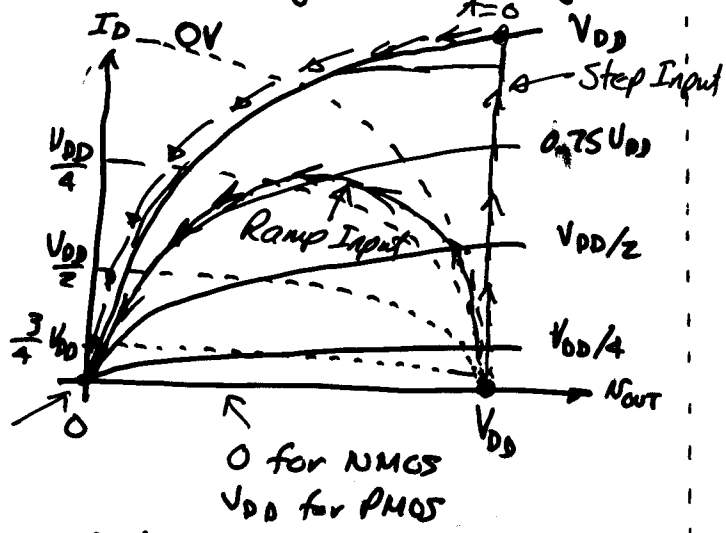
$C_{wire} = (0.2 fF/\mu m) \times (\text{Length of the conductor})$



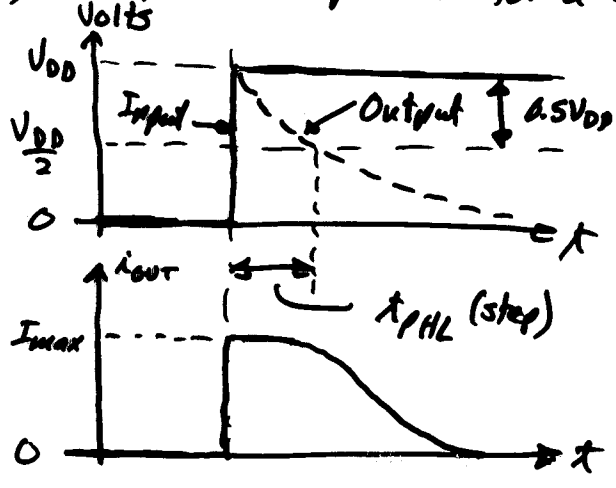
So far, all inputs have been step inputs.

Improving the Delay Calculations including the input stage





1.) Analytical Expression for a Delay with a Step Input

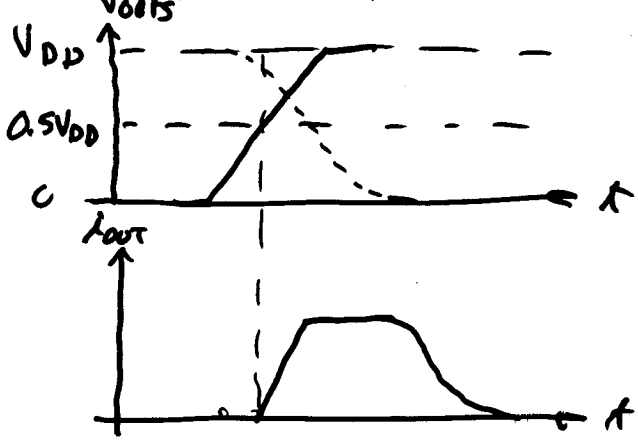


$$i_{out} \approx i_{max} = C_L \frac{dV_{out}}{dt}$$

$$i_{OUT} = C_L \frac{\Delta V}{\Delta t} = C_L \frac{0.5V_{DD}}{t_{pHL}(step)}$$

$$t_{pHL}(step) = C_L \frac{V_{DD}}{2 i_{max}}$$

2.) Analytical Expression for a Delay with a Ramp Input



$$t_{pHL}(ramp) = \frac{t_r}{4} + t_{pHL}(step)$$