Capacitance of NMOS

\[ C_{load} = C_{self} = \frac{C_{G1} + C_{G2} + C_{G3} + C_{S3} + C_{G4}}{5} \]

\[ C_{load} = C_{eff}(W_n) + C_{eff}(W_p) + C_{eff}(W_p) \]

\[ = C_{eff} \left[ W_n + 2W_p \right] = 9W \times C_{eff} = 9W \times (1 \text{fF/\mu m}) \]

\[ C_{in} \text{ (worst case)} = C_g(W_n + W_p) = SW \times C_g = 5W \times (2 \text{ fF/\mu m}) \]

**NAND3 Example**

Find \( C_{M} \) (worst case) and \( C_{load} \) if \( W = 0.4 \mu m \).

\[ C_{M} \text{ (worst case)} = C_g(W_n + W_p) = SW \times C_g = 5 \times (0.4) \times (5 \text{ fF/\mu m}) \]

\[ C_{load} = C_{self} \left[ 2W_p + 3W_n \right] = (1 \text{ fF/\mu m}) \times (9W + 9W) = 18 \times (0.4) \times (1) = 52 \text{ fF} \]
Switching Implications on Gates from a Speed Viewpoint

In a series logic stack, the delay from the input to the output increases the further away a transistor is from the output.

Suppose the following circumstances:
1. A is late, only $C_L$ needs to be charged.
2. If B is late, both $C_X$ and $C_L$ must be charged.
3. If C is late, the $C_L + C_X + C_Y$ must be charged.

Move a transistor with a delayed input closest to the output.

Wiring Capacitance

$$C_{wire} = (0.2 \text{fF/\mu m}) \times \text{(Length of the Conductor)}$$
So far, all inputs have been step inputs.

Improving the Delay Calculations including the input stage

1) Analytical Expression for a Delay with a Step Input

\[ i_{\text{out}} = i_{\text{max}} = C \frac{dV_{\text{out}}}{dt} \]

\[ i_{\text{out}} = C \frac{dV}{dt} = C \frac{Q_{\text{VDD}}}{k_{\text{VH}}(\text{step})} \]

\[ k_{\text{VH}}(\text{step}) = C \frac{V_{\text{DD}}}{2i_{\text{max}}} \]

2) Analytical Expression for a Delay with a Ramp Input

\[ k_{\text{H}}(\text{ramp}) = \frac{\Delta t}{Q} + k_{\text{H}}(\text{step}) \]