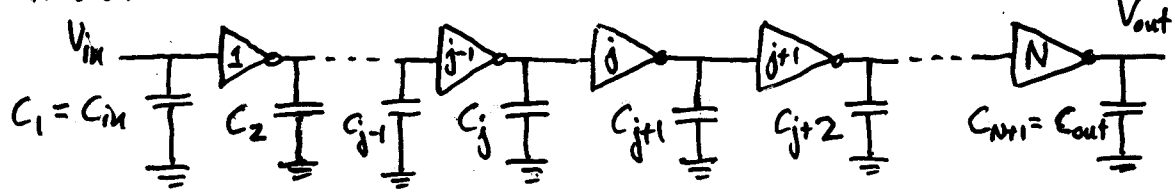
Review of Gate Sizing for Optimal Path Delay

Problem:



$$\text{Total delay} = \sum_{j=1}^{N} \tau_{inv}\left(\frac{C_{j+1}}{C_j} + \gamma_{inv}\right) \qquad \gamma_{inv} = \frac{C_{self}}{C_{in}}$$

$0.5 < \gamma_{inv} < 2$

Optimal sizing occurs when,

$$W_j = (W_1 W_2 \cdots W_{j-1} W_{j+1} \cdots W_{N-1} W_N)^{1/N}$$

This leads to a fanout for each inverter of $f_j = \frac{W_{j+1}}{W_j} = f$

$$\therefore \text{Total Delay} = N \times \tau_{inv}\left(\frac{C_j}{C_{j-1}} + \gamma_{inv}\right) = \frac{\ln\left(\frac{C_{out}}{C_{in}}\right)}{\ln f} \times \tau_{inv}\left(f + \gamma_{inv}\right)$$

Example 6.9 (Again)

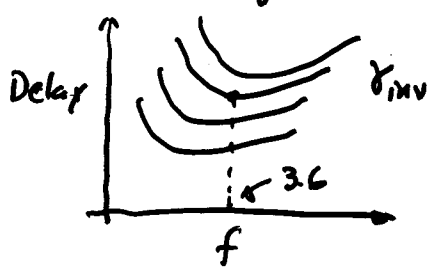
1.) Find the optimal fanout for $N=3$ and the total delay if $C_{out} = 200fF$ and $C_{in} = 1fF$. Assume $\tau_{inv} = 7.5ps$ and $\gamma_{inv} = 0.5$

$$\ln f = \frac{\ln\left(\frac{C_{out}}{C_{in}}\right)}{N} = \frac{\ln 200}{3} = 1.766 \rightarrow f = 5.85$$

$$\text{Total delay} = 3(7.5ps)(5.85 + 0.5) = 143ps$$

2.) Find the optimal N and the delay for this case.

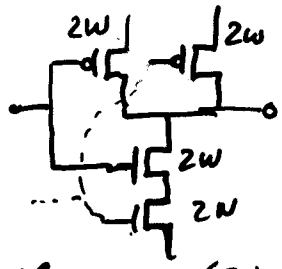
From Fig 6.23, $f \approx 3.6 \rightarrow N = \frac{\ln(200)}{\ln(3.6)} = 4.13 \rightarrow N = 4$



$$\text{Total delay} = 4(7.5ps)[3.6 + 0.5] = 123ps$$

Optimizing Paths with NANDs, NORs, and Combinations

1.) NAND2

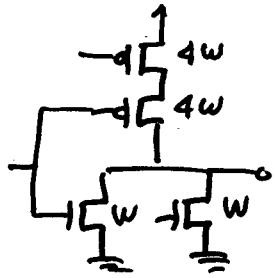


$$\text{Total delay} = \sum_j \tau_{nand}\left(\frac{C_{j+1}}{C_j} + \gamma_{nand}\right)$$

$$\tau_{nand} = R_{eff} C_{in} = R_{eqn}\left(\frac{L_n}{W_n}\right) C_g 4W_n = 4R_{eqn} C_g L_n \quad \text{(2 inputs)}$$

$f_{opt} \approx 4$

2.) NOR2



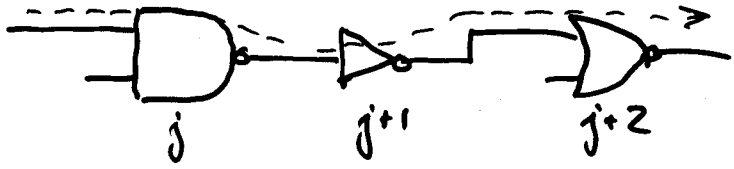
$$\text{Total delay} = \sum_j \tau_{NOR}\left(\frac{C_{j+1}}{C_j} + \gamma_{NOR}\right)$$

$$\tau_{NOR} = R_{eff} C_{in} = R_{eqn}\left(\frac{L_n}{W_n}\right) 5W_n C_g$$

$$= 5R_{eqn} C_g L_n$$

$f_{opt} \approx 4$

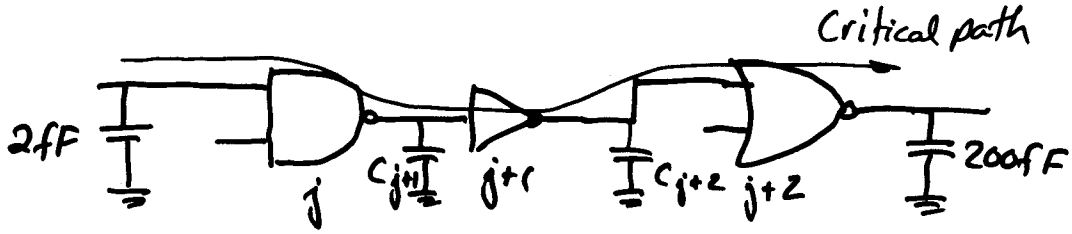
3.) Combinations of gates



The delay is minimized when $\tau \times FO$ of a given gate is equal to $\tau \times FO$ of the next gate, regardless of the type of gate.

Example of Computing Optimal Gate Sizes along a Critical Path

Find the device sizes that optimize the delay thru the path shown below.



We know for optimum delay that,

$$\tau_{nand}\left(\frac{C_{j+1}}{2fF}\right) = \tau_{inv}\left(\frac{C_{j+2}}{C_{j+1}}\right) = \tau_{nor}\left(\frac{200fF}{C_{j+2}}\right)$$

$$\therefore \text{Fanout delay} = \sqrt[3]{\tau_{nand}\left(\frac{C_{j+1}}{2fF}\right)\tau_{inv}\left(\frac{C_{j+2}}{C_{j+1}}\right)\tau_{nor}\left(\frac{200fF}{C_{j+2}}\right)}$$

$$= \sqrt[3]{\tau_{nand}\cdot\tau_{inv}\cdot\tau_{nor}\left(\frac{200}{2}\right)} = \sqrt[3]{4\tau_{inv}\cdot 3\tau_{inv}\cdot 5\tau_{inv}\,(100)}$$

$$= \tau_{inv}\sqrt[3]{4\cdot 3\cdot 5\cdot 100} = \tau_{inv}\,18.17 = 18.17\,\underbrace{R_{eqn}C_g L_n}_{\tau_{inv}}$$

C_{j+2}:

$$\tau_{nor}\left(\frac{C_{load}}{C_{j+2}}\right) = 5R_{eqn}C_g L_n\left(\frac{200fF}{C_{j+2}}\right) = 18.19\,R_{eqn}C_g L_n \quad (\times 18.2)$$

$$C_{j+2} = \frac{5\,(200fF)}{18.2} = 55fF = 5W_nC_g$$

$$W_n = \frac{55}{5.2} = 5.5\mu m \rightarrow W_p = 4W_n = 22\mu m$$

C_{j+1}:

$$\tau_{inv}\left(\frac{C_{j+2}}{C_{j+1}}\right) = 3R_{eqn}C_g L_n\left(\frac{55fF}{C_{j+1}}\right) = 18.2\,R_{eqn}C_g L_n$$

$$C_{j+1} = \frac{3\cdot 55}{18.2} = 9.1fF = 3W_nC_g \rightarrow W_n \approx 1.5\mu m$$

$$W_p = 2W_n = 3\mu m$$

C_{in}: $\tau_{nand}\left(\frac{C_{j+1}}{C_{in}}\right) = 4R_{eqn}C_{gn}\left(\frac{9.1fF}{C_{in}}\right) = 18.2R_{eqn}C_{gn}$

$C_{in} = \frac{4 \cdot 9.1}{18.2} = 2fF = 4W_nC_g \rightarrow W_n = 0.25\mu m$

$W_p = W_n = 0.25\mu m$

Optimizing the Paths using Logical Effort

Logical Effort?

$$\text{Logical effort} = LE = \frac{\text{Total delay}}{\tau_{inv}}$$

General path -

$$LE = \frac{\text{Total Delay}}{\tau_{inv}} = \frac{\tau_{nand}}{\tau_{inv}}\left(\frac{C_{j+1}}{C_j} + \gamma_{nand}\right) + \frac{\tau_{inv}}{\tau_{inv}}\left(\frac{C_{j+2}}{C_{j+1}} + \gamma_{inv}\right)$$

$$+ \frac{\tau_{nor}}{\tau_{inv}}\left(\frac{C_{j+3}}{C_{j+2}} + \gamma_{nor}\right)$$

⋮