OPTIMIZING PATHS USING LOGICAL EFFORT

Logical "Effort"

$$\text{Logical effort} = LE = \frac{\text{Total Delay}}{\tau_{inv}}$$

For a general path,

$$LE = \frac{\text{Total Delay}}{\tau_{inv}} = \frac{\tau_{nand}}{\tau_{inv}}\left(\frac{C_{j+1}}{C_j} + \gamma_{nand}\right) + \frac{\tau_{inv}}{\tau_{inv}}\left(\frac{C_{j+2}}{C_{j+1}} + \gamma_{inv}\right) + \frac{\tau_{nor}}{\tau_{inv}}\left(\frac{C_{j+3}}{C_{j+2}} + \gamma_{nor}\right)$$

or in normalized form,

$$D = (LE_{nand} \cdot FO_1 + p_{nand}) + (LE_{inv} \cdot FO_2 + p_{inv}) + (LE_{nor} \cdot FO_3 + p_{nor})$$

where $LE_{gate} = \frac{\tau_{gate}}{\tau_{inv}}$, $FO_j = \frac{C_{j+1}}{C_j}$, and $p_{gate} = LE_{gate} \cdot \gamma_{gate}$

Gate LE (LE_{gate}):

$$\tau_{inv} = 3R_{eqn}C_gL_n, \quad \tau_{nand2} = 4R_{eqn}C_gL_n \text{ \& } \tau_{nor2} = 5R_{eqn}C_gL_n$$

$$LE_{inv} = 1, \quad LE_{nand2} = \frac{4}{3}, \quad LE_{nor2} = \frac{5}{3}$$

n-input gates –

$$LE_{nandn} = \frac{n+2}{3} \text{ \& } LE_{norn} = \frac{2n+1}{3} \quad \text{(Table 6.1)}$$

Parasitic term, p:

$$p_{inv} = LE_{inv} \times \gamma_{inv} = LE \times \frac{C_{self}}{C_{in}} = LE \times \frac{C_{eff}3W}{C_g 3W} = LE \times \frac{C_{eff}}{C_g} = \frac{1}{2}$$

$$p_{nand2} = LE_{nand} \times \frac{C_{self}}{C_{in}} = LE_{nand} \times \frac{C_{eff}(2W+2W+2W)}{C_g(2W+2W)} = \frac{4}{3}\left(\frac{1}{2}\right)\left(\frac{3}{2}\right) = 1$$

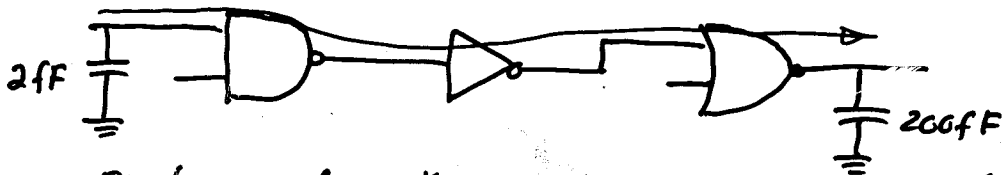
$$p_{nor\text{-}2} = LE_{nor\text{-}2} \times \frac{C_{self}}{C_{in}} = LE_{nor\text{-}2} \times \frac{C_{eff}(W+4W+4W)}{C_g(W+4W)} = \left(\frac{5}{3}\right)\left(\frac{9}{5}\right)\left(\frac{1}{2}\right) = \frac{3}{2}$$

Parasitic P - cont'd

For n-inputs

$$P_{nand-n} = \frac{n}{2} \quad \text{and} \quad P_{nor-n} = \frac{3n}{4} \quad \text{(Table 6.2)}$$

Example - Path Optimization using Logical Effort



First, equalize the LE×FO components of delay for all gates.

$$\text{Total path efforts} = LE_{nand}\left(\frac{C_{j+1}}{2ff}\right) \times LE_{inv}\left(\frac{C_{j+2}}{C_{j+1}}\right) \times LE_{nor}\left(\frac{200fF}{C_{j+2}}\right)$$

$$= \left(\frac{4}{3}\right)\left(\frac{C_{j+1}}{2ff}\right)(1)\left(\frac{C_{j+2}}{C_{j+1}}\right)\left(\frac{5}{3}\right)\left(\frac{200fF}{C_{j+2}}\right) = \left(\frac{4}{3}\right)(1)\left(\frac{5}{3}\right)\left(\frac{200}{2}\right)$$

$$= 222.2$$

$$\text{Gate effort} = \text{Stage Effort} = (\text{Total path effort})^{1/n} = \sqrt[3]{222.2} = 6$$

$$\text{Normalized delay} = D = (LE_{nand} \cdot FO_{nand} + P_{nand}) + (LE_{inv} \cdot FO_{inv} + P_{inv}) + (LE_{nor} \cdot FO_{nor} \cdot P_{nor})$$

But all we know is that

$$LE_{nand} \cdot FO_{nand} = LE_{inv} \cdot FO_{inv} = LE_{nor} \cdot FO_{nor} = 6$$

$$\therefore \quad D = 3(LE \cdot FO) + P_{nand} + P_{inv} + P_{nor} = 3 \cdot 6 + 1 + \frac{1}{2} + \frac{3}{2}$$

$$D = 21$$

Minimum path delay $= 21\,\tau_{inv} = 21(7.5ps) = 157.5ps$

Design the W values for each gate:

Work backwards to compute the W's

$$LE_{nor}\left(\frac{C_{out}}{C_{j+2}}\right) = 6 \quad \leftarrow \quad C_{j+2} = \frac{5}{3}\,\frac{200}{6} = 55fF$$

$LE_{inv}\left(\frac{C_{j+2}}{C_{j+1}}\right)=6 \rightarrow C_{j+1}=0)\frac{55ff}{6}=9.1ff$

$LE_{nand}\left(\frac{C_{j+1}}{2ff}\right)=6 \rightarrow 2ff \stackrel{?}{=} \frac{4}{3}\frac{9.1ff}{6}\simeq 2ff$

Logical effort can also be used to size the gates.

Example of Finding D for Fig 5.8

NAND4 - INV - NAND2 - INV:

Let $C_L=200ff$ and $C_{in}=2ff$

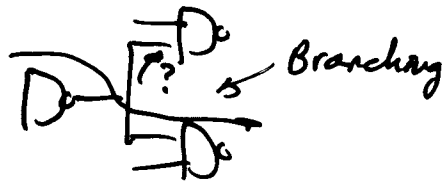
$$D=4(\text{Path effort})^{1/4}+\sum_{i=1}^{4}P_i$$

$$D=4\left(\frac{6}{3}\cdot 1\cdot\frac{4}{3}\cdot\frac{1}{1}\cdot\frac{10}{1}\right)^{1/4}+\left(2+\frac{1}{2}+1+\frac{1}{2}\right)=9+4=13$$

NAND2 - NOR2 - NAND2 - INV:

$$D=4\left(\frac{4}{3}\cdot\frac{5}{3}\cdot\frac{4}{3}\cdot 1\cdot\underbrace{10}_{\frac{C_L}{C_{in}}}\right)^{1/4}+\left(1+\frac{3}{2}+1+\frac{1}{2}\right)=9.33+4=13.33$$

Branching Effort and Sideloads



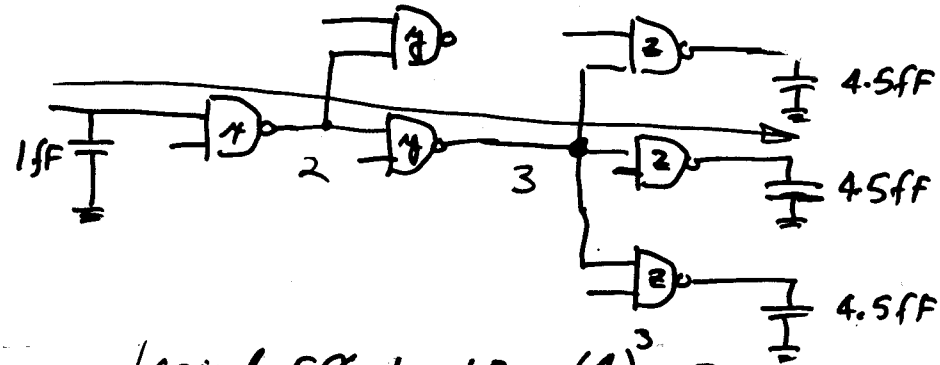
For similar branches we can write,

Total path effort $=\Pi(LE\times BE\times FO)=\Pi(LE\times BE)\times\frac{C_{load}}{C_{in}}$

where BE = branching factor = no. of identical loads

Example

Select the gate sizes (y and z) to minimize delay in the path shown –



Logical Effort = $LE_p = \left(\frac{4}{3}\right)^3 = 2.37$

Electrical effort = $FO_p = \frac{C_{out}}{C_{in}} = 4.5$

Branching effort = $BE_p = (2)(3) = 6$

Path effort = $PE = (LE_p)(FO_p)(BE_p) = 64$

Optimal stage Effort = $SE^* = PE^{1/3} = 4$

Delay = $D = N \cdot SE^* + Parasitics = 3 \cdot 4 + 3(1) = 15$

Using $(LE_j)(BE_j)\left(\frac{C_{j+1}}{C_j}\right) = 4$ solve for C_z, C_y & C_x

$\left(\frac{4}{3}\right)(1)\left(\frac{4.5}{C_z}\right) = 4 \rightarrow C_z = \left(\frac{4}{3}\right)\left(\frac{4.5}{4}\right) = 1.5fF$

$\left(\frac{4}{3}\right)(3)\left(\frac{1.5}{C_y}\right) = 4 \rightarrow C_y = \left(\frac{4}{3}\right)(3)\left(\frac{1.5}{4}\right) = 1.5fF$

$\left(\frac{4}{3}\right)(2)\left(\frac{1.5}{C_x}\right) = 4 \rightarrow C_x = \left(\frac{4}{3}\right)(2)\left(\frac{1.5}{4}\right) = 1fF$

(we already knew C_x but this checks the work)

Sideloads –

Case where one of the loads is known. The approach is:

1.) Solve ignoring the sideload

2.) Add sideload and remove gates beyond the sideload.

3.) Combine the two solutions