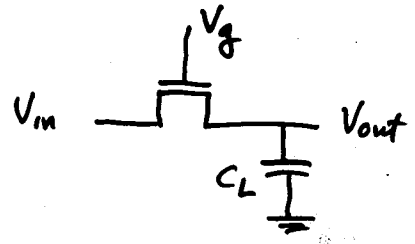
CHAPTER 7- TRANSFER GATE AND DYNAMIC LOGIC DESIGN

Pass Transistors (switches)

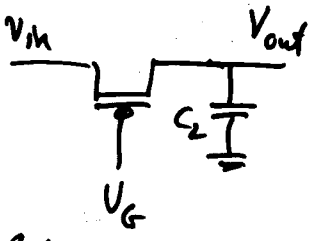
1.) NMOS



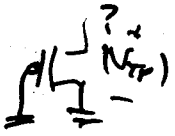
V_G	V_{in}	V_{out}
0	0	Hi Z
0	V_{DD}	Hi Z
V_{DD}	0	0
V_{DD}	V_{DD}	$V_{DD}-V_{TN}$

The NMOS works best when V_{in} & V_{out} are close to ground.

2.) PMOS



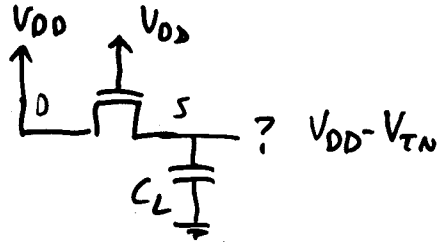
V_G	V_{in}	V_{out}
0	0	$\lvert V_{TP}\rvert$
0	V_{DD}	V_{DD}
V_{DD}	0	Hi Z
V_{DD}	V_{DD}	Hi Z



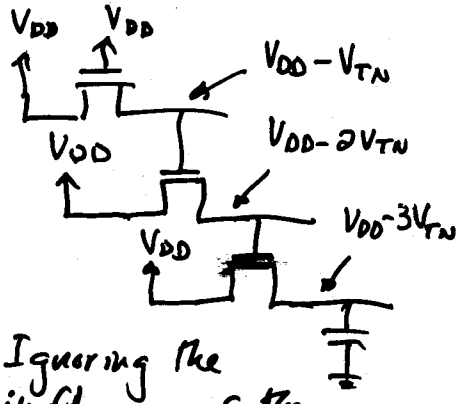
The PMOS works best when V_{in} & V_{out} are close to V_{DD}.

Some Examples

1.)

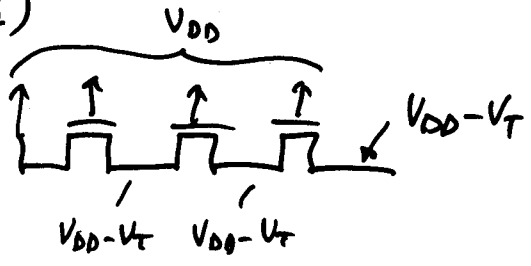


2.)



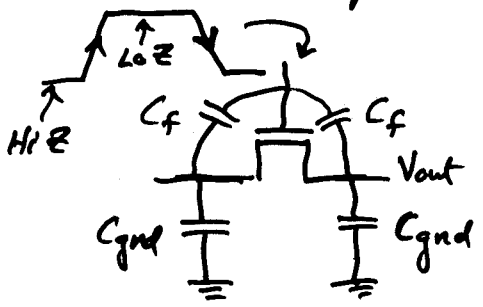
Ignoring the influence of the balks.

3.)

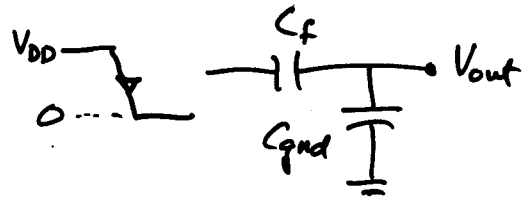


Capacitive Feedthrough (Clock feedthrough)

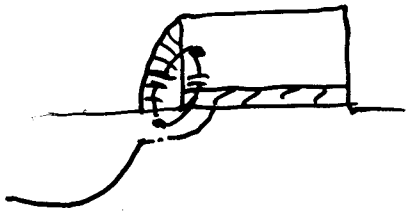
Capacitive feedthru occurs when the clock on the gate is switching the MOS to the hi-Z state.

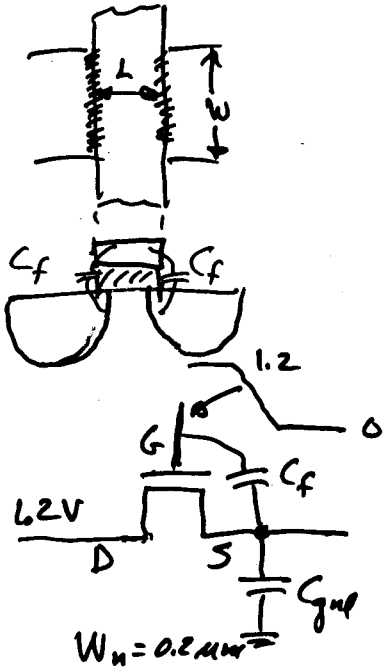


C_f = overlap capacitance $= C_{OL} = C_{ox} \cdot LD \cdot W$



$$V_{out} = V_{out}(ON) - V_{DD}\frac{C_f}{C_f + C_{gnd}}$$





Example

In the circuit shown with the input at 1.2V, what is the initial value of the output when the clock is 1.2V? Estimate the final value of V_{out} after the clock goes low. Assume 0.13 μm technology.

1.) $V_{TN} = 0.4 + 0.2\sqrt{0.88 + V_{out}} - 0.2\sqrt{V_{out}}$

(γ, γ, 24p)

$V_{out} = 1.2 - V_{TN}$ ⟵ Use iteration ⟵ $V_{TN} = 0.483 \Rightarrow V_{out} \approx 0.72$ V

2.) $C_f = C_{ox} \cdot LD \cdot W = \left(1.6\frac{fF}{cm^2}\right)\left(10^{-7}\,cm\right)\left(0.2\times10^{-4}\,cm\right) = 0.032\,fF$

(LD: 10 nm, W: 0.2 μm)

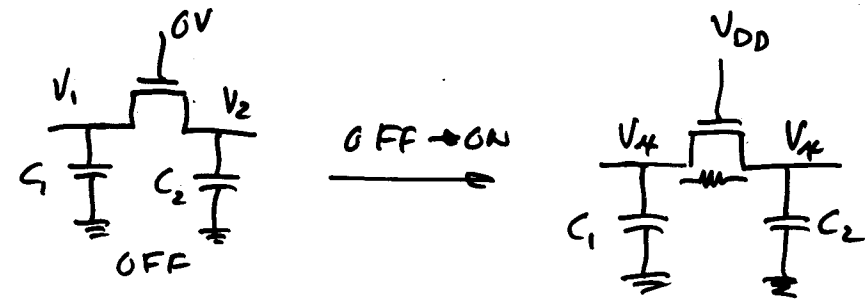
$C_{gnd} = C_{eff} \times W = \left(1\frac{fF}{\mu m}\right)(0.2\,\mu m) = 0.2\,fF$

Example - Cont'd

$$V_{out} = 0.72V - 1.2\left(\frac{0.032}{0.032+0.2}\right) = 0.716 - 0.166 \cong 0.55V$$

Charge Sharing

Illustration -



$Q_{total} = C_1V_1 + C_2V_2$ $\qquad$ $Q_{total} = V_M(C_1+C_2)$

$$\therefore V_M(C_1+C_2) = C_1V_1 + C_2V_2 \rightarrow V_M = \frac{C_1}{C_1+C_2}V_1 + \frac{C_2}{C_1+C_2}V_2$$

Example:

Compute the charge-sharing effects for the following cases using 0.13 μm technology.

a.) $C_1 = 100fF$, $C_2 = 20fF$, $V_1 = 0$, $V_2 = 1.2V$

$$V_X = \frac{100fF \cdot 0 + 20fF \cdot 1.2V}{120fF} = 0.2V$$

b.) $C_1 = 20fF$, $C_2 = 20fF$, $V_1 = 0$, $V_2 = 1.2V$ → $V_X = 0.6V$

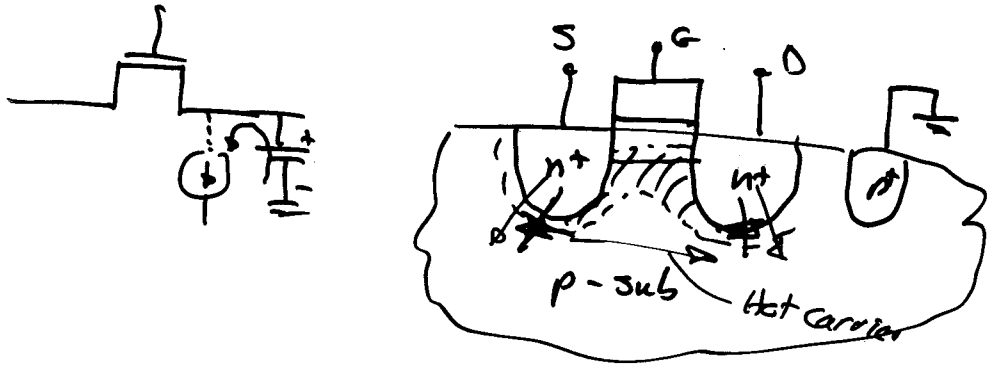
c.) $C_1 = 20fF$, $C_2 = 100fF$, $V_1 = 0$, and $V_2 = 1.2V$

$$V_X = \frac{20fF \cdot 0 + 100fF \cdot 1.2}{120fF} = 1V$$

Whoops - The maximum voltage is $V_{DD} - V_{TN} = 0.8V$

Other Sources of Charge Loss

1.) Leakage current from BD and BS pn junctions.



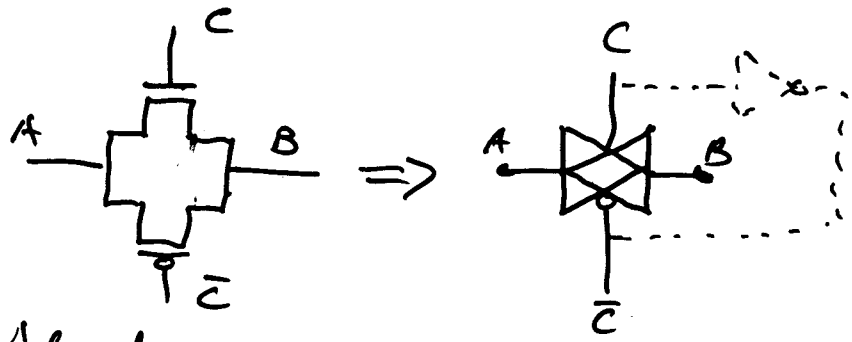
2.) Noise injection

a.) Electrostatic or electromagnetic (noise on power supply)

b.) Hot carriers → substrate

c.) α-particles

CMOS Transmission Gate



Advantages –

Can transmit either a high or low

Cancellation of clock feedthrough (somewhat)

Disadvantages –

Requires more transistors

Requires $\overline{\text{CLOCK}}$