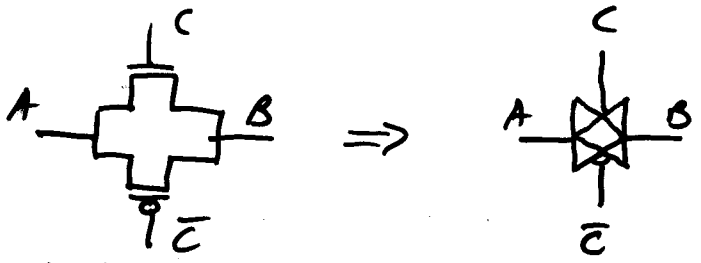
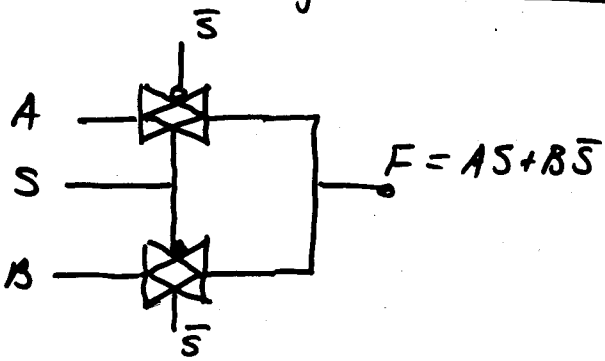
Transmission Gate

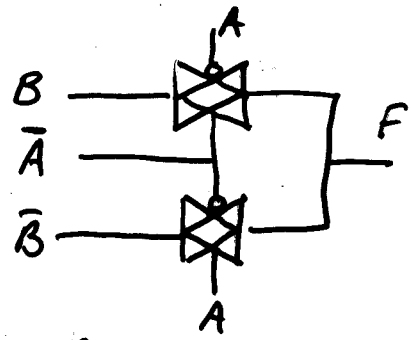


C=1 T.G. is ON
C=0 T.G. is OFF

Multiplexers Using CMOS Transfer Gates



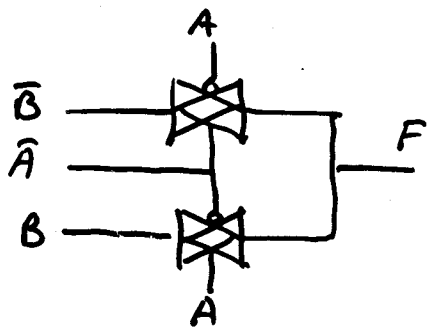
XOR Gate



$F = A\bar{B} + \bar{A}B = A \oplus B$

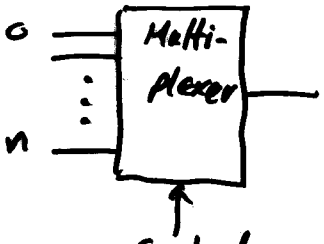
(6 transistors compared with 16 for static logic)

XNOR Gate

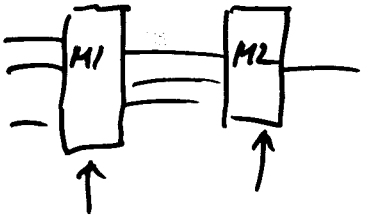


$F = AB + \bar{A}\bar{B} = \overline{A \oplus B}$

Multiplexer -



One level



Two-level multiplexer

Tradeoffs between single and multiple-level MUXs

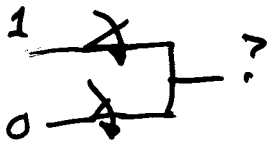
Single has less control signals, quicker

Multiple has less inverter (logic) → Less area

Slower

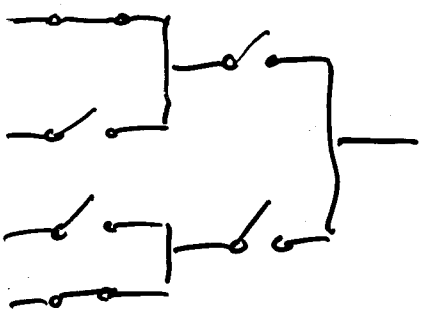
Output conflicts for MUXs

1.) Two defined paths conflict

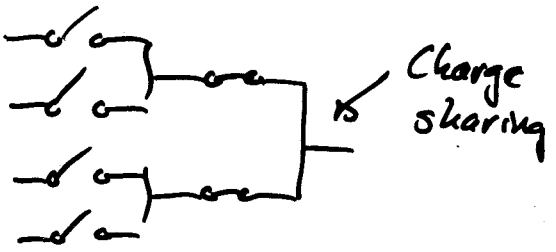


2.) No defined paths

Hi Z state



3.) Charge sharing



Implemeation of Logic Functions

1.) Identify the control signals
2.) Build truth table
3.) Convert the truth table to a multiplexer-style design by creating a path for each row to the output.
4.) The desire outputs are routed from input to the output.

Example 1

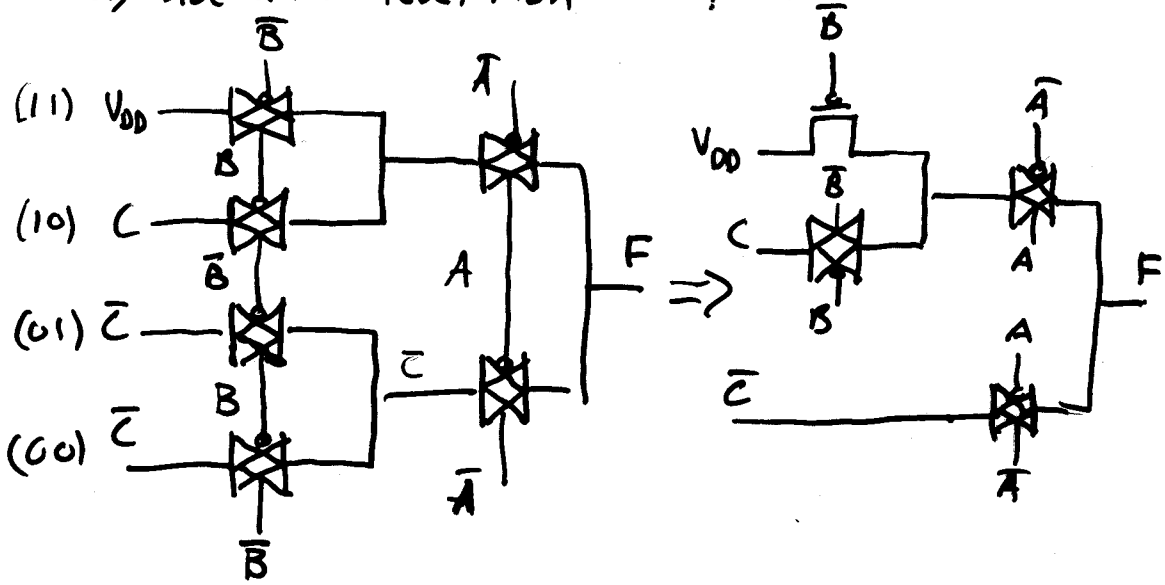
$F = AB + A\bar{B}C + \bar{A}\bar{C}$

1.) Let A & B be the control signals.

2.)

A	B	F
0	0	$\bar{C}$
0	1	$\bar{C}$
1	0	C
1	1	1

3.) Use a two-level MUX



Note that you can also combine TGs and static logic gates for efficient implementation of logic functions

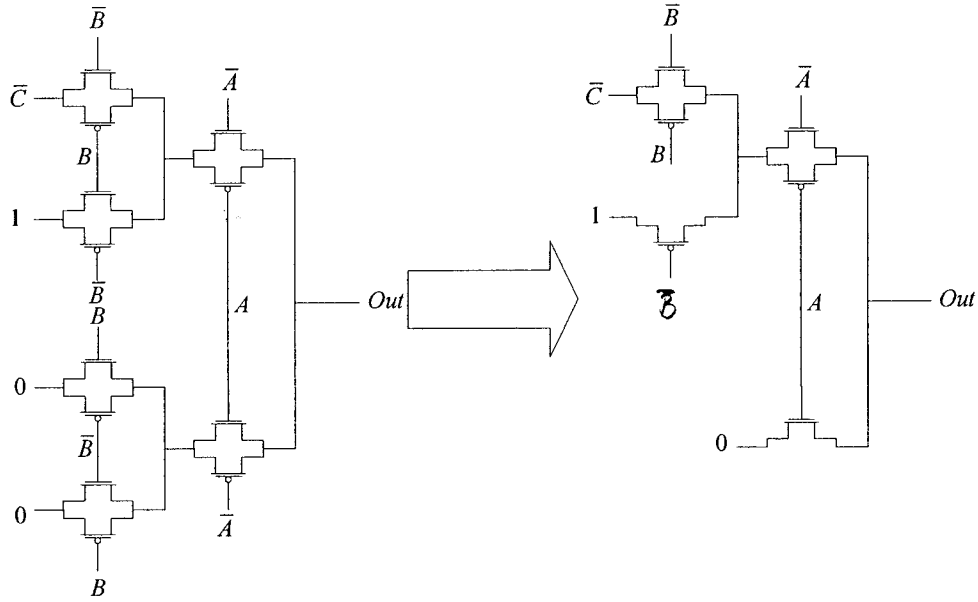
Problem 7.4 (c)

$Out = \overline{(A+B+C)} + \bar{A}B = \bar{A}\bar{B}\bar{C} + \bar{A}B$

Let A and B be the control signals

A	B	C	Out
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

A	B	OUT
0	0	1
0	1	1
1	0	0
1	1	0

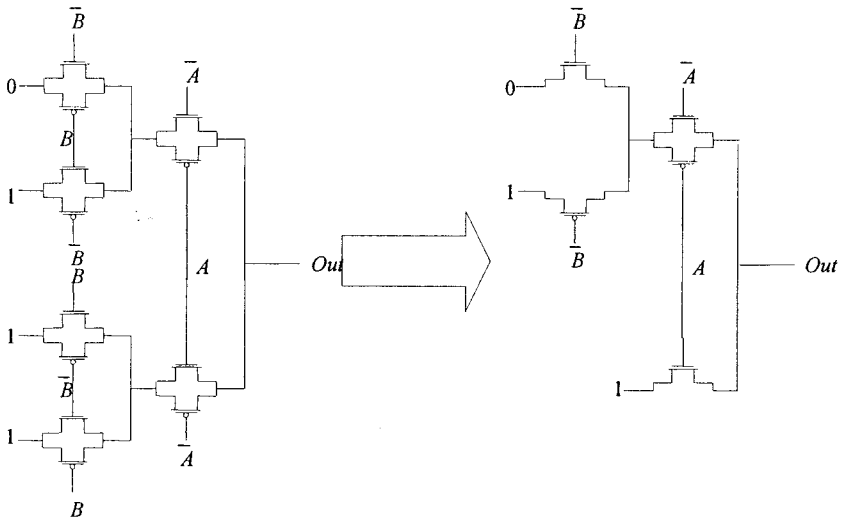


Problem 7.4(b)

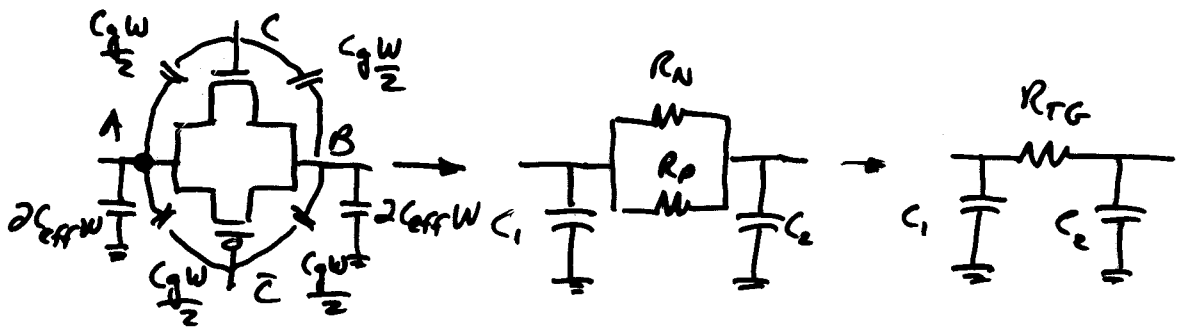
$$Out = \overline{\overline{\left(A + B + \overline{C}\right)} + \overline{A}\overline{B}} = \overline{\overline{A}\overline{B}C + \overline{A}\overline{B}} = \overline{\overline{A}\overline{B}\left(C + 1\right)} = \overline{\overline{A}\overline{B}} = A + B$$

A	B	C	Out
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

A	B	OUT
0	0	0
0	1	1
1	0	1
1	1	1



CMOS TG Delays



Delay = RC

R = ?

1.) For the propagation of a V_{DD}, (30K / 12.5K)

$$R_{TG} = R_N \| R_P = 2R_{eqn} \| R_{eqp} = 2R_{eqn} \| 2.4R_{eqn} \approx 1.1R_{eqn} \approx R_{eqn}$$

2.) For the propagation of a 0, (Approx. PMOS as twice the normal resistance)

$$R_{TG} = R_N \| R_P \cong R_{eqn} \| 4.8R_{eqn} = 0.83 \approx R_{eqn}$$

Bottom line: $R \simeq R_{eqn}$.

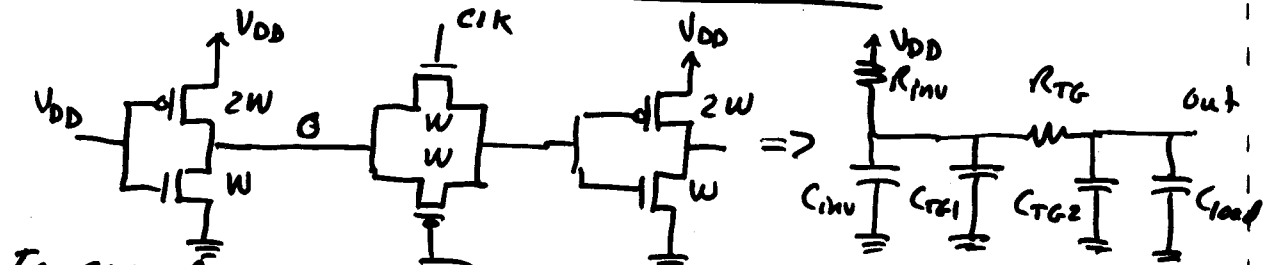
C = ?

1.) Off state: $C_1 = C_2 = C_{in} = C_{out} = C_{eff}(W_n + W_p) = 2W C_{eff}$

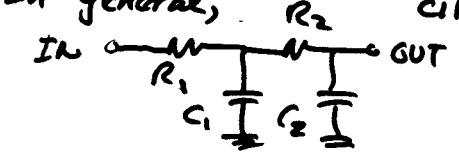
2.) ON state: $C_1 = C_2 = C_{eff}(W_n + W_p) + \frac{1}{2}(C_g W_n + C_g W_p)$

$$= 2C_{eff}W + WC_g$$

Transmission Gate with a Driver and a Load



In general,



Elmore's Delay -

$$t_{Elmore} = R_1C_1 + (R_1+R_2)C_2 + (R_1+R_2+R_3)C_3 + \cdots$$