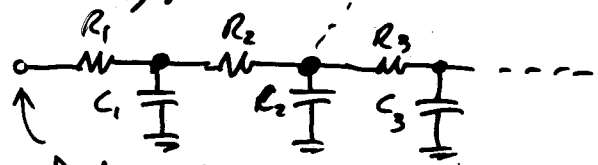
Exam #3 scheduled for 4/16/04 has been moved to 4/14/04.
Conflicts: Contact Dr. Allen by e-mail before 4/14.

Transmission Gates combined with Inverter (Driver)—

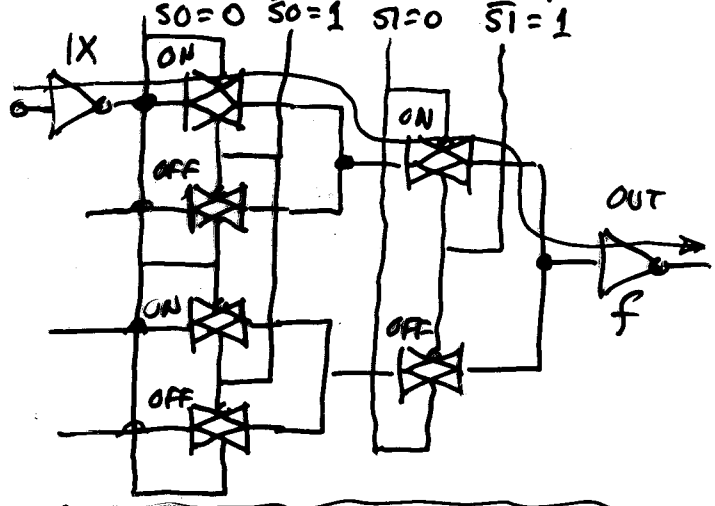
Elmore Delay:



Delay at input = $R_1C_1 + (R_1+R_2)C_2 + (R_1+R_2+R_3)C_3 + \cdots$

Ex. 7.4

Find the Elmore delay for the path shown where the fanout of 1X inverter at the output of the MUX is f.



$t_1 = R_{inv}C_1 + (R_{inv}+R_{TG})C_2 + (R_{inv}+2R_{TG})C_3$

$R_{inv} = R \quad R_{TG} = R$

$C_1 = 3WC_{eff} + 2WC_{eff} + WC_g$

$C_1 = 5WC_{eff} + WC_g$

$C_2 = 2(2WC_{eff} + WC_g) + 2WC_{eff}$

$= 6WC_{eff} + 2WC_g$

$C_3 = 3WfC_g + 2WC_{eff} + WC_g + 2WC_{eff}$

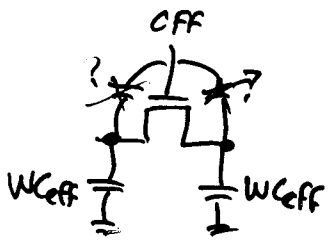
$C_3 = 4WC_{eff} + WC_g(1+3f)$

Review:

OFF TG: $C_{in} = 2WC_{eff}$

ON TG: $C_{in} = 2WC_{eff} + \frac{1}{2}C_gW + \frac{1}{2}C_gW$

$= 2WC_{eff} + WC_g$



$t_1 = RW[5C_{eff} + 2C_g] + 2RW[6C_{eff} + 2C_g] + 3RW[4C_{eff} + C_g + 3fC_g]$

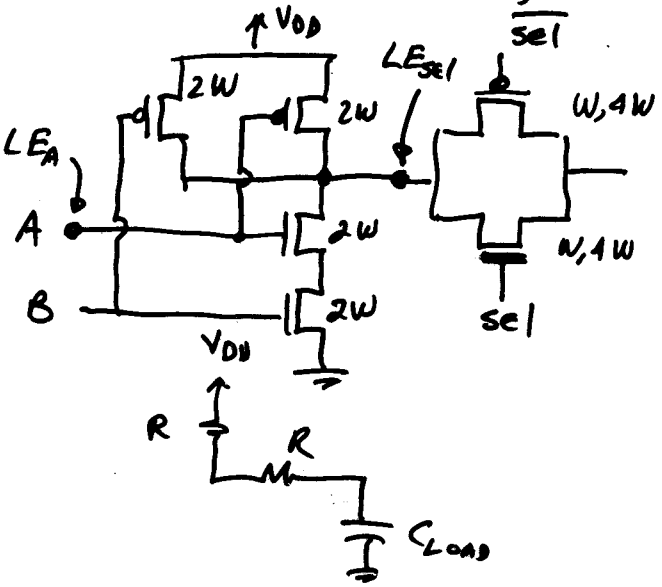
$t_1 = RW[29C_{eff} + 8C_g + 9fC_g]$

Logical Effort for CMOS TG's

Recall that $LE = \frac{\tau_{gate}}{\tau_{inv}} = \frac{\tau_{gate}}{3WRC_g}$ $\quad \tau = (\text{Pullup } R)(\text{Input } C)$

Example 7.5

Compute the LE_A and LE_{sel} for the NAND gate shown which drives a TG with a.) Width of TG = W & b.) Width of TG = 4W.



W:

$$LE_A = \frac{\tau_{gate}}{3WRC_g} = \frac{2R(4WC_g)}{3WRC_g} = \frac{8}{3}$$

$$LE_{sel} = \frac{2R(WC_g)}{3WRC_g} = \frac{2}{3}$$

4W:

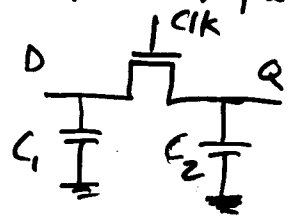
$$LE_A = \frac{4WC_g\left(R+\frac{R}{4}\right)}{3WRC_g} = \frac{5}{3}$$

$$LE_{sel} = \frac{WC_g\left(R+\frac{R}{4}\right)}{3WRC_g} = \frac{5}{3}$$

DYNAMIC D-LATCHES AND D FLIP-FLOPS

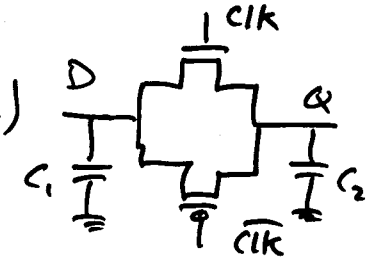
Evolution of Simple D-Latches using TGs

1.)



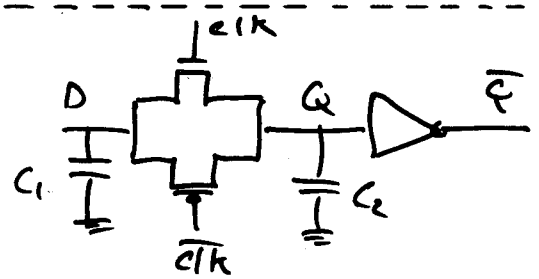
Problems:
- Propagation of V_{DD}
- Clock feedthru
- No $\bar{Q}$ available
- Output is hi-Z when clk goes low

2.)



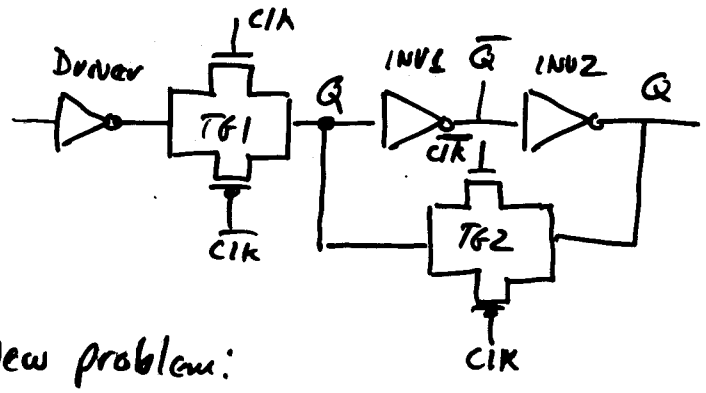
Solves:
- Propagation of V_{DD}
- Somewhat solves the clock feedthru

3.)



Solves the no $\bar{Q}$ problem

4.)



New problem:

When CLK goes high, the delay before $\overline{CLK}$ goes low can cause a conflict at Q between TG1 and TG2

Solution 1: Size the gates so that the forward path is stronger than the feedback path.

Solution 2: