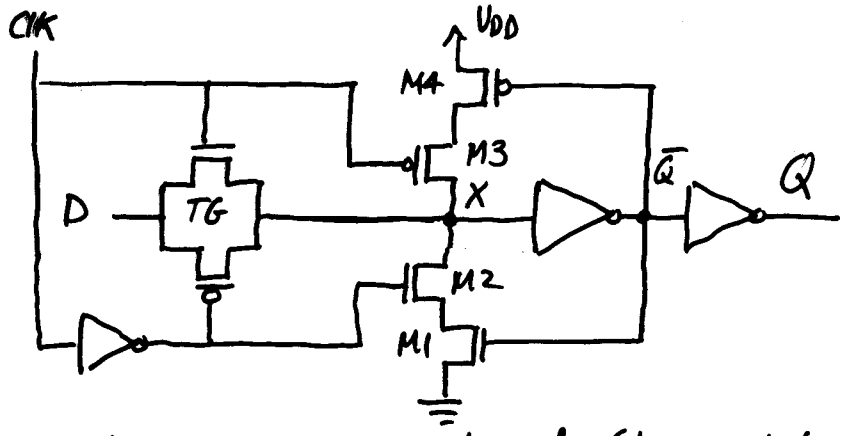
Solution to the internal node conflict for the simple D-latch –



Clk = 1 : Transparent mode (has a delay of TG + 2·INV)

D=0: → $\bar{Q}$ = 1 (M1 ON, M2 OFF, M3 OFF, M4 OFF)

D=1: → $\bar{Q}$ = 0 (M1 OFF, M2 OFF, M3 OFF, M4 ON)

Clk = 0 : Hold mode (latch mode)

D=0: → $\bar{Q}$ = 1 (M1 ON, M2 ON, M3 ON, M4 OFF)

D=1: → $\bar{Q}$ = 0 (M1 OFF, M2 ON, M3 ON, M4 ON)

Master-Slave D Flip-Flop

(See next page)

Domino Logic

Evolution –

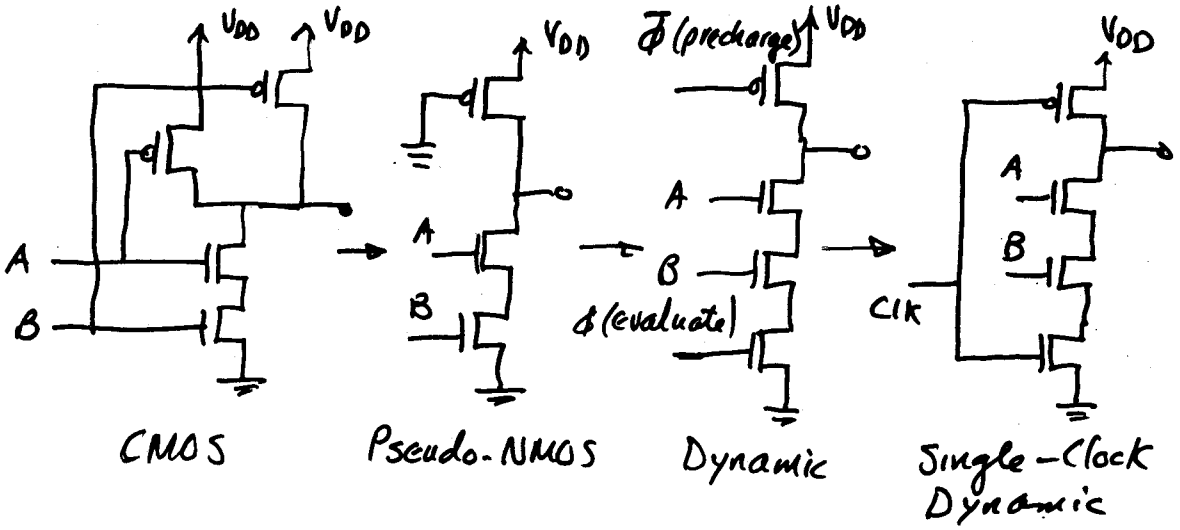
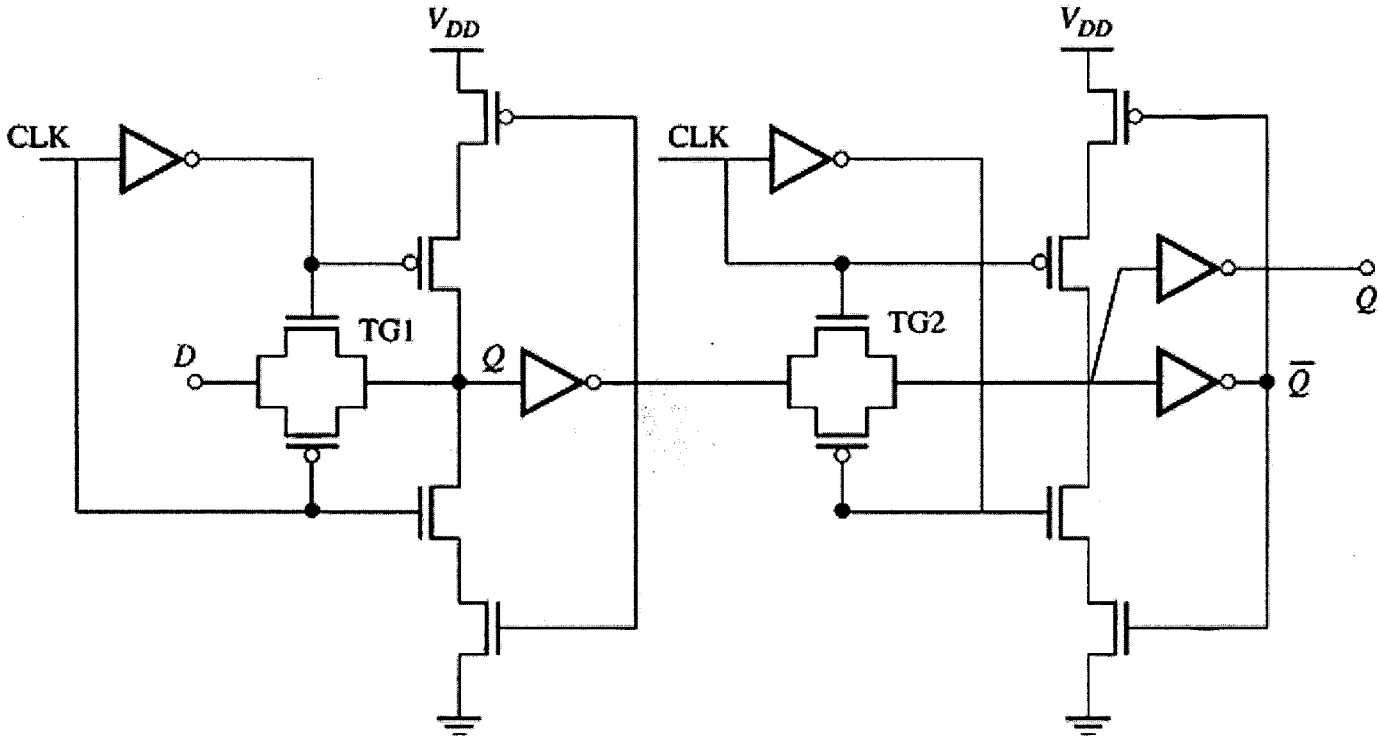
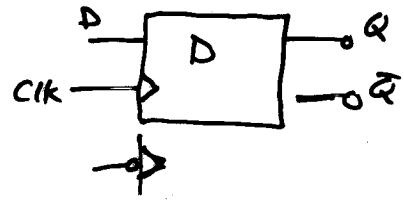


Figure 7.24 – Positive edge-triggered D-type flip-flop



Positive edge of the CLK shuts off the first latch and enables the second.

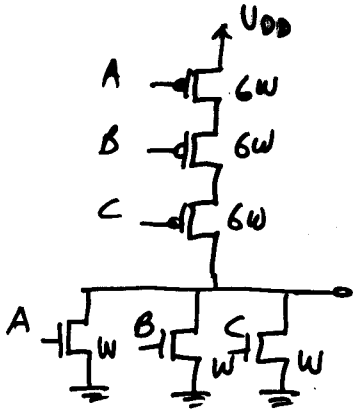


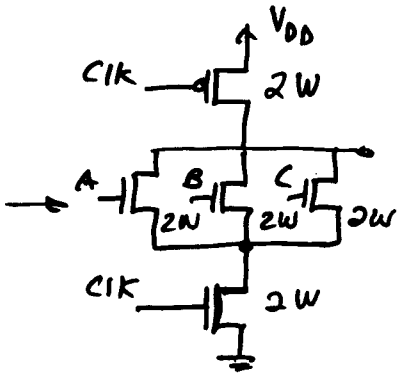
Clk=0 : 1st latch is transparent
2nd latch is disabled

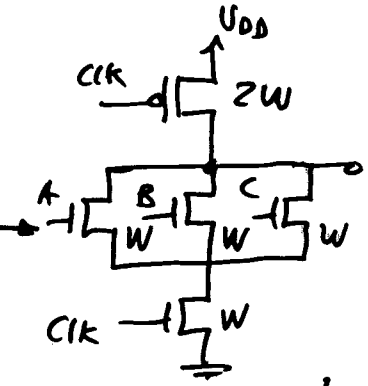
Clk=1 : TG1 shuts off and holds D at its output (of 1st latch)
TG2 allows Q to flow to the output.

Since D is only transmitted to the output on the rising edge of the clock, this ff is positive edge triggered.

3-input Dynamic NOR gate

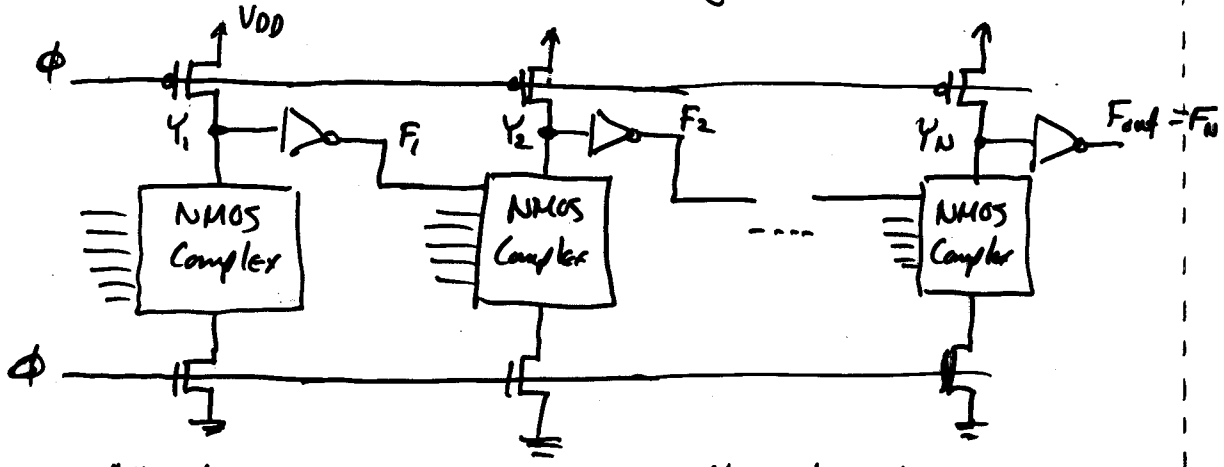






If the Clk arrives before A, B, or C.

General structure of a dynamic gate -



All stages are precharged to V_{DD} when $\phi = 0$

When $\phi = 1$, the internal nodes will change from left to right assuming that there is a path to ground thru the various NMOS complexes

Domino Logic - Some Observations

1.) Since the output is already high, we can speed up the gate by increasing the sizes of the NMOS transistors

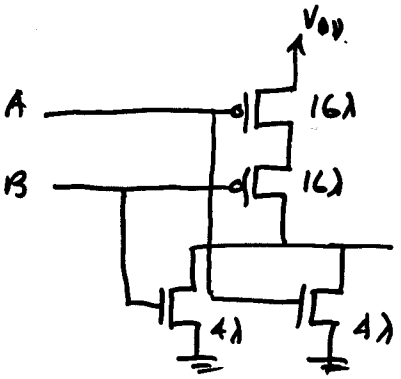
2.) Since there is no pull-up fighting the pull down a domino stage will actually switch faster than a regular gate.

3.) Power savings - only those gates that discharge the output node to ground will dissipate power.

4.) Domino logic can only be used to create a non-inverting logic function.

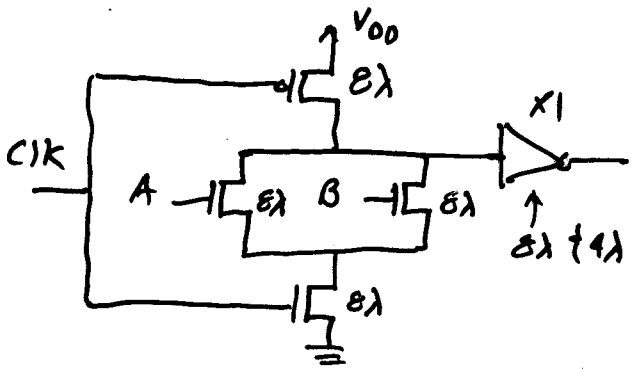
Logic Effort for Domino Gates

Static NOR2 with a dynamic (domino) NOR2 —



$L = 2\lambda$

Static NOR2



Dynamic NOR2

$$LE_{NOR} = \frac{\text{NOR input C}}{\text{INV input C}}$$

$$= \frac{20\lambda}{12\lambda} = \frac{5}{3} = 1.67$$

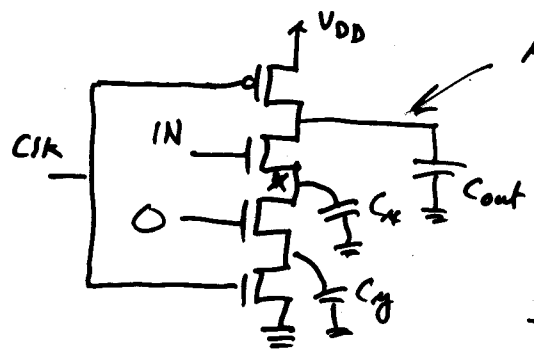
$$LE_{Dyn\,NOR} = \frac{\text{Dynamic Input C}}{\text{INV input C}} = \frac{8\lambda}{12\lambda} = \frac{2}{3}$$

$$LE_{INV} = 1$$

$$\therefore LE_{Domino} = \sqrt{LE_{Dyn.\,NOR} \cdot LE_{INV}} = 0.8$$

Limitations of Domino Logic

1.) Charge sharing



As IN goes from 0 → 1,

$$V_{out} = V_{DD} - \underbrace{\frac{C_{out}}{C_x + C_{out}} V_{DD}}$$

$$0\,C_x + C_{out} V_{DD} = V_p (C_x + C_{out})$$

If $C_x = C_{out}$, then $V_{out} = \frac{V_{DD}}{2}$

Solutions:

1.) Increase Cout ???

2.) Precharge node X to V_{DD}

3.) Use keepers

2.) Leakage