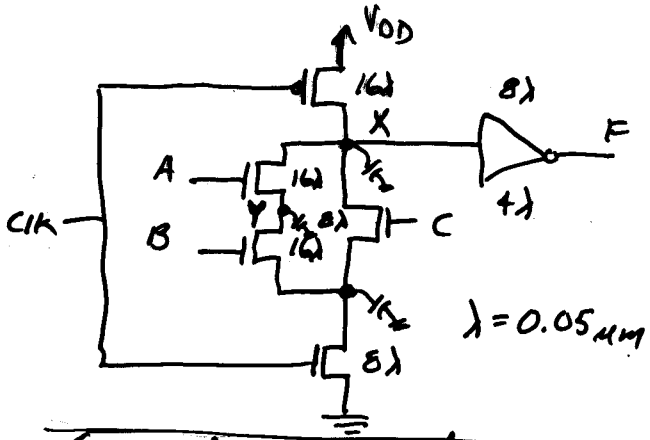
Example 7.8 - Continued



1.) What logic function does the gate perform?

2.) How much clock feedthru is observed at node X?

3.) What is the worst-case charge sharing at node X?

The worst case charge sharing occurs for the output at 1.2V and A = 1 and B = C = 0.

$C_Y = (1fF/\mu m)(16\lambda) = \frac{1fF}{\mu m}(16)(0.05\mu m)$

$= 0.8fF$

∴ Charge sharing between nodes X and Y ($C_X = 3.2fF$), is

$V^* = \frac{C_X}{C_X + C_Y} \times 1.2 = \frac{3.2}{4.0} \times 1.2 = 0.96V$

Problem: The maximum voltage at Y is $1.2 - 0.4 = 0.8V$

Consequently, the rest of the charge is at node X

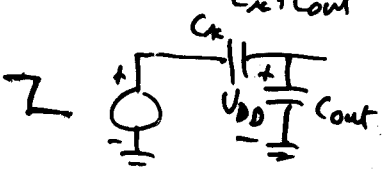
$(3.2fF)(1.2V) - (0.8fF)(0.8V) = 3.84fC - 0.64fC = 3.2fC$

$\therefore V_X = \frac{3.2fC}{3.2fF} = 1V$

Comment of last lecture -

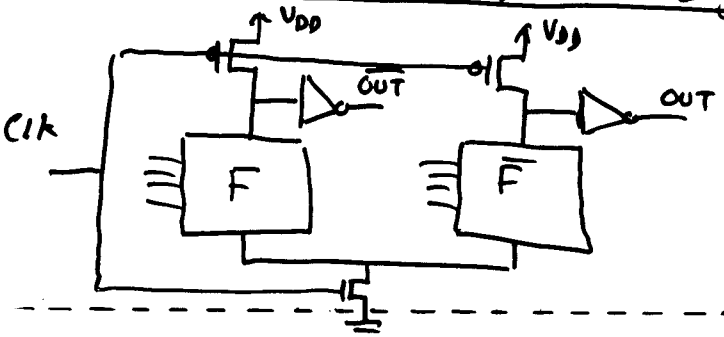
$\Delta V_{out} = \cancel{V_{DD}} - \frac{C_{out}}{C_{ext}+C_{out}} V_{DD}$

$V_{out} = \frac{C_{out}}{C_{ext}+C_{out}} V_{DD}$



Solution #7 have been changed

Dual-Rail (Differential) Domino Logic

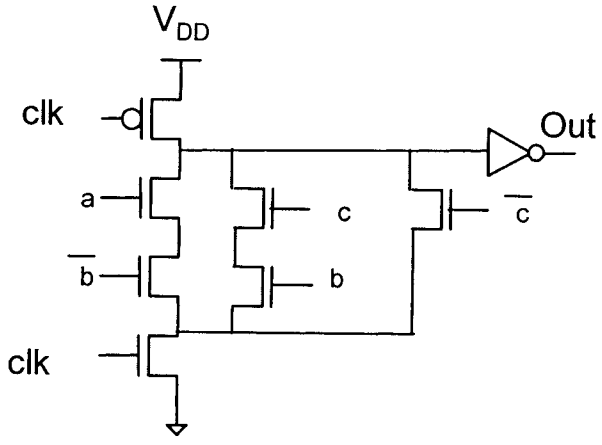


Achieve both a inverting and noninverting logic.

P7.6b

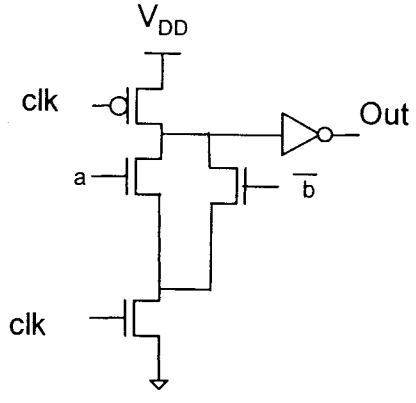
Examples of Designing Domino Logic

1.) $Out = A\overline{B} + BC + \overline{C}$

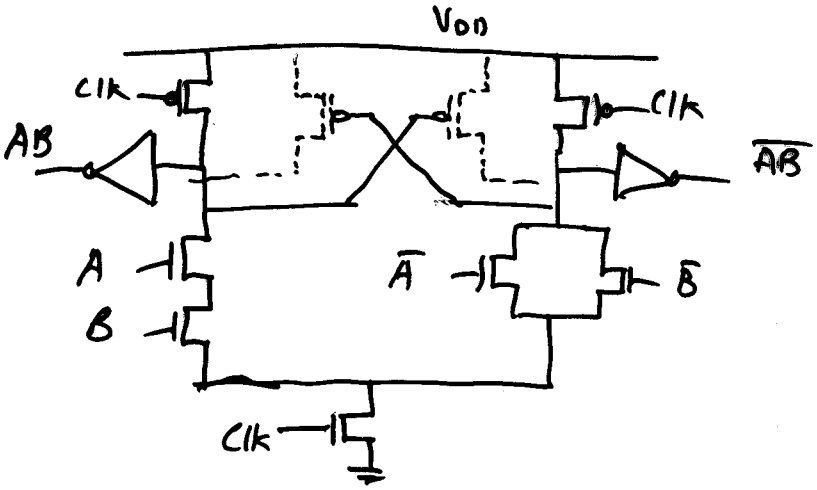


P7.6d

2.) $Out = \overline{\overline{(A + \overline{B} + C)} + \overline{A}B} = (A + \overline{B} + C)(A + \overline{B}) = A + \overline{B}$



NAND Differential Domino Logic Example



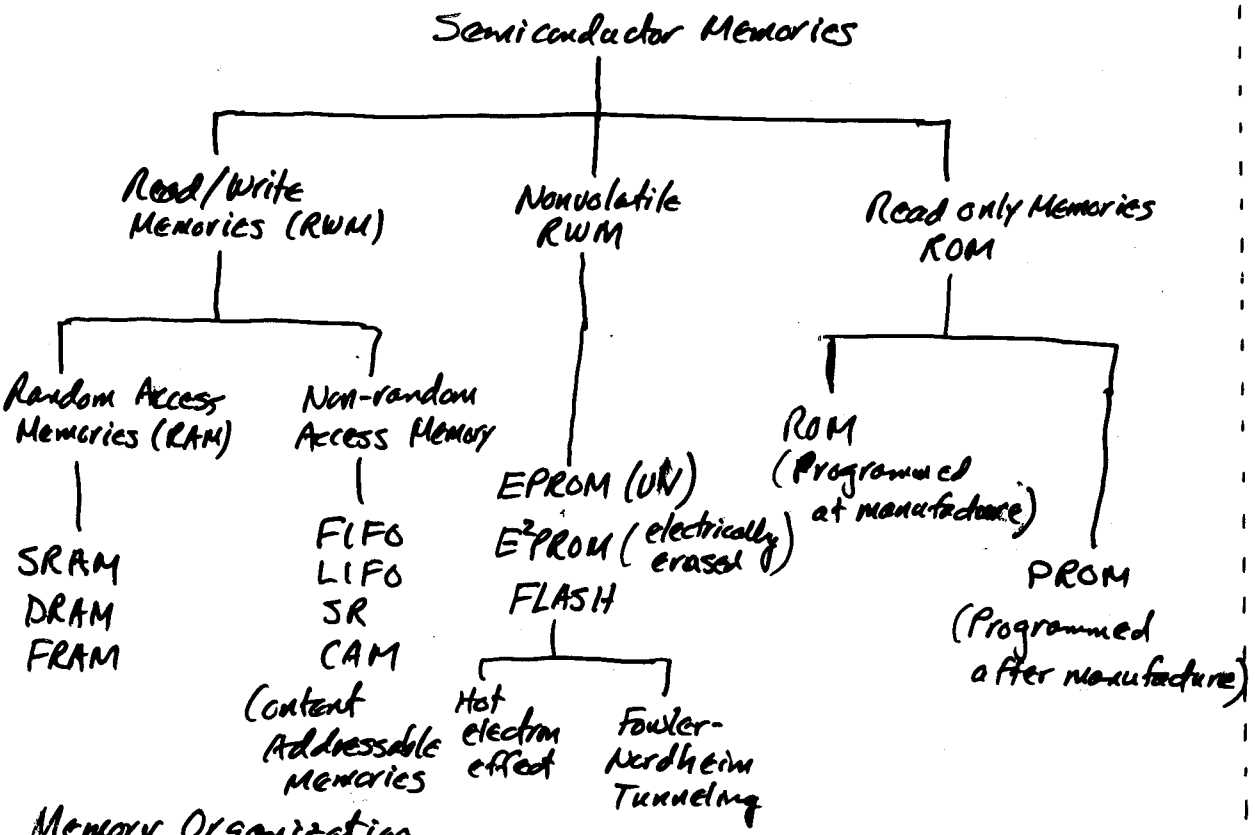
CHAPTER 8 - SEMICONDUCTOR MEMORY DESIGN

Introduction

- Memories are ckts. or systems that store digital information in large quantity.
- Size of memories ranges from 100 bits to over 256 M bits
- Units of size

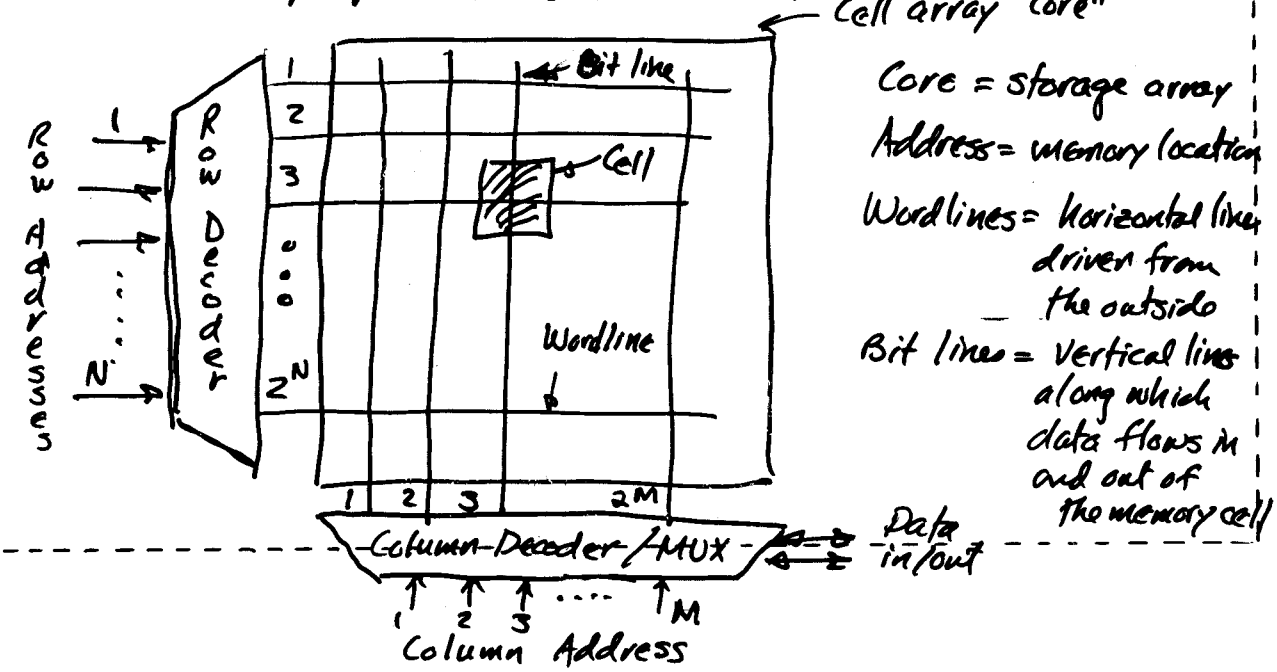
  Bit = Digital 1 or 0 (flip-flop or similar ckt.)
  Byte = 8 bits (a single alphanumeric character)
  Word = 32 to 128 bits

Memory Classification –



Memory Organization

- Non random access – FIFO, LIFO, shift register, etc.
- Random access – the memory locations can be accessed in a random or fixed order independent of the physical location for the purpose of read or write.

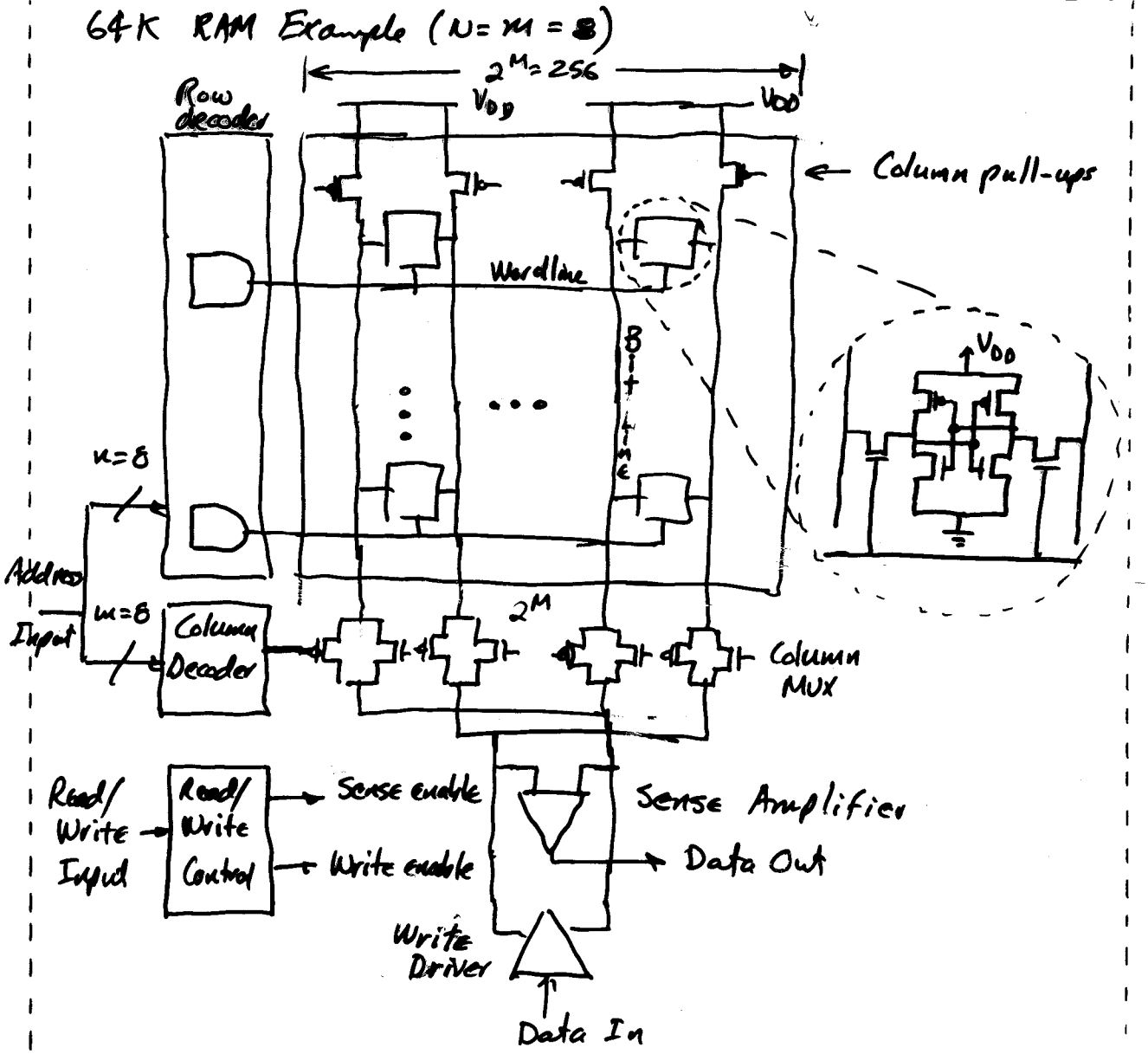


Core = storage array

Address = memory location

Wordlines = horizontal lines driven from the outside

Bit lines = vertical lines along which data flows in and out of the memory cell


64K RAM Example (N = M = 8)
$2^M = 256$
Row decoder
V_{DD}
V_{DD}
Column pull-ups
Wordline
Bit line
V_{DD}
n=8
Address Input
m=8
Column Decoder
2^M
Column MUX
Read/ Write Input
Read/ Write Control
Sense enable
Write enable
Sense Amplifier
Data Out
Write Driver
Data In