## Memory Organization

(See Fig. 8.2)

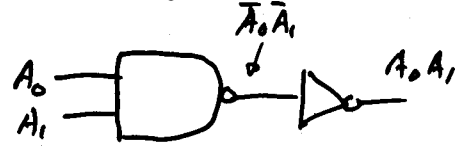
## MOS Decoders

Two-stage decoder =

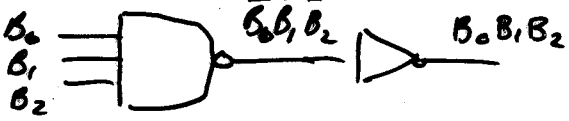
An n-bit decoder require $2^n$ logic gates each with n-inputs

For example if n=6 → 64 gates driving 64 inverters

First-stage (predecoder)




Second-stage -




Two level Decoder for a 6-bit address — (Fig. 8.6)

## Example 8.1 - Decoder Sizing use LE Techniques

Size the decoder for n=6 case using FO4 rules assuming that the normalized output loading is 1.

For each stage, $C_{in} = \frac{LE \times BE \times C_{out}}{4}$

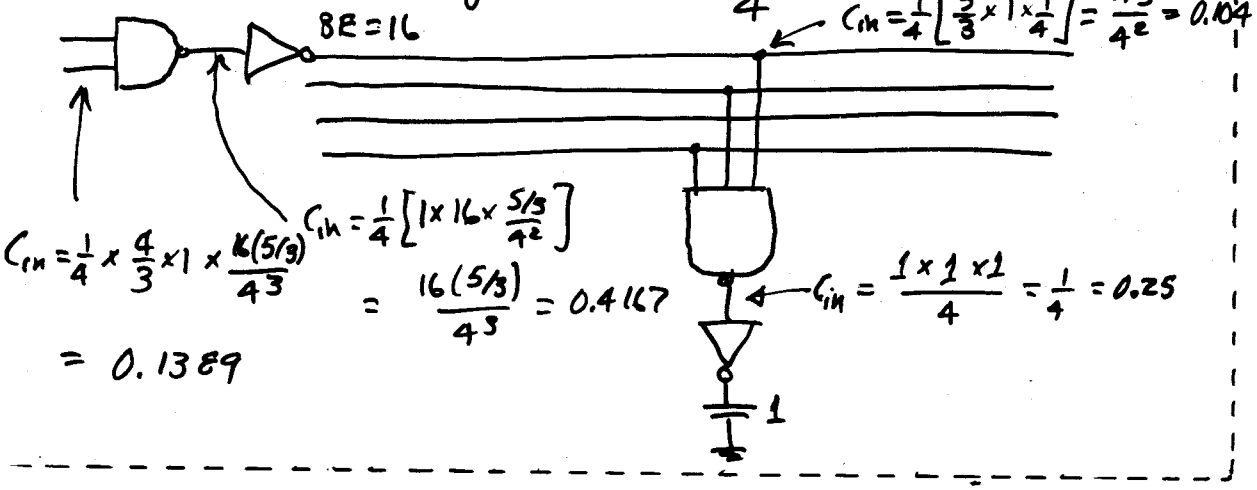
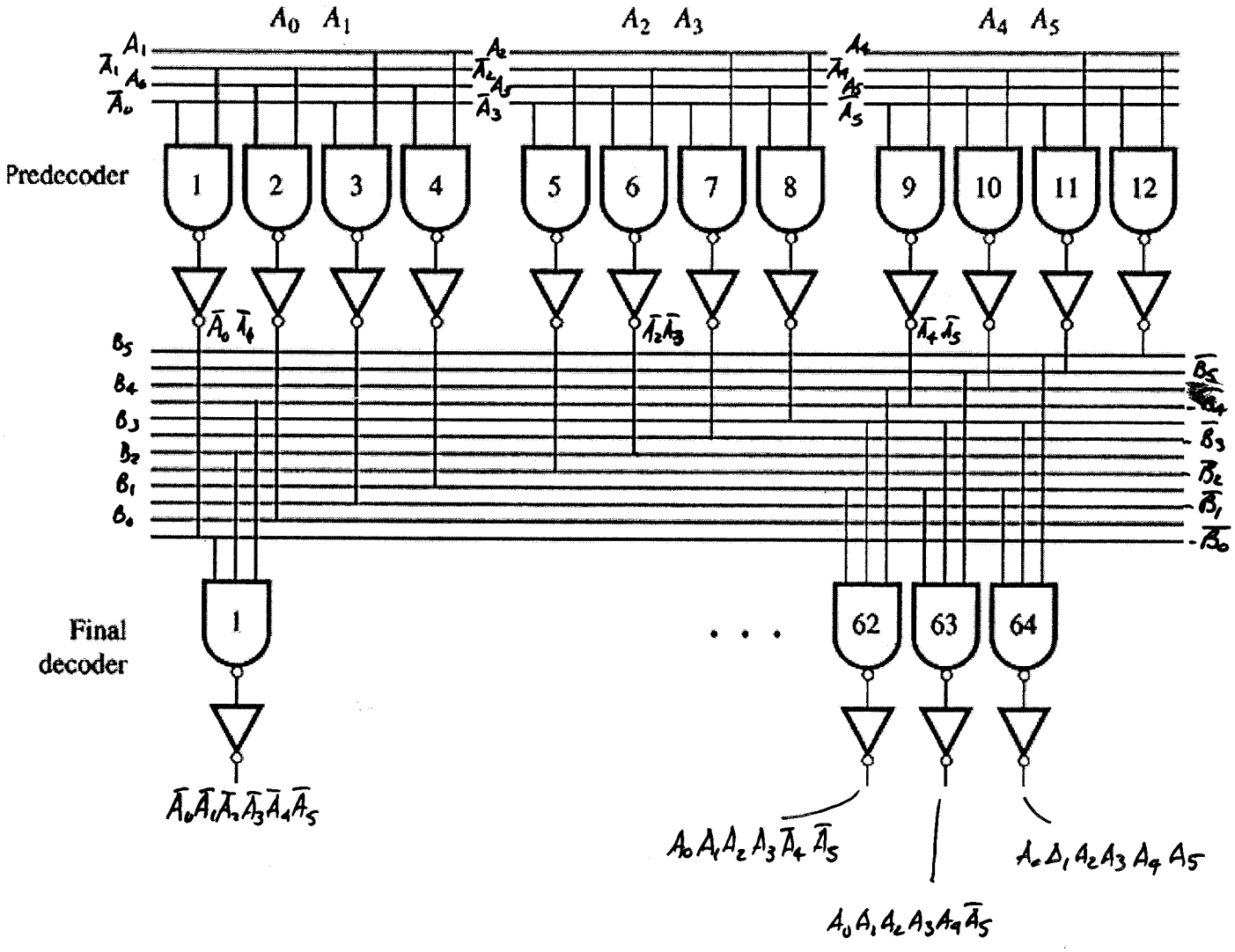
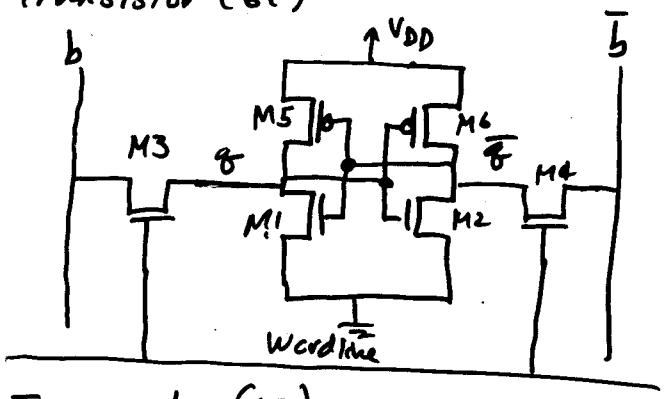


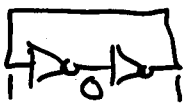
**Figure 8.6 – Structure of two-level decoder for 6-bit address**



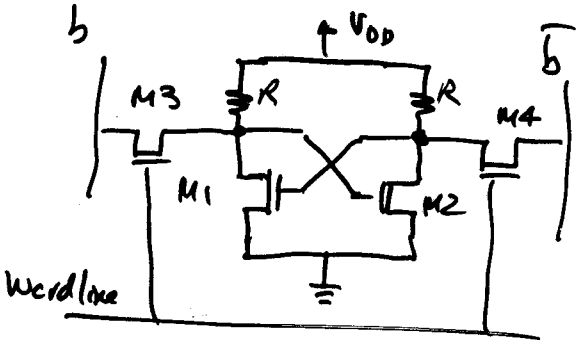
# Static RAM Cell Design

## 6 Transistor (6T) –



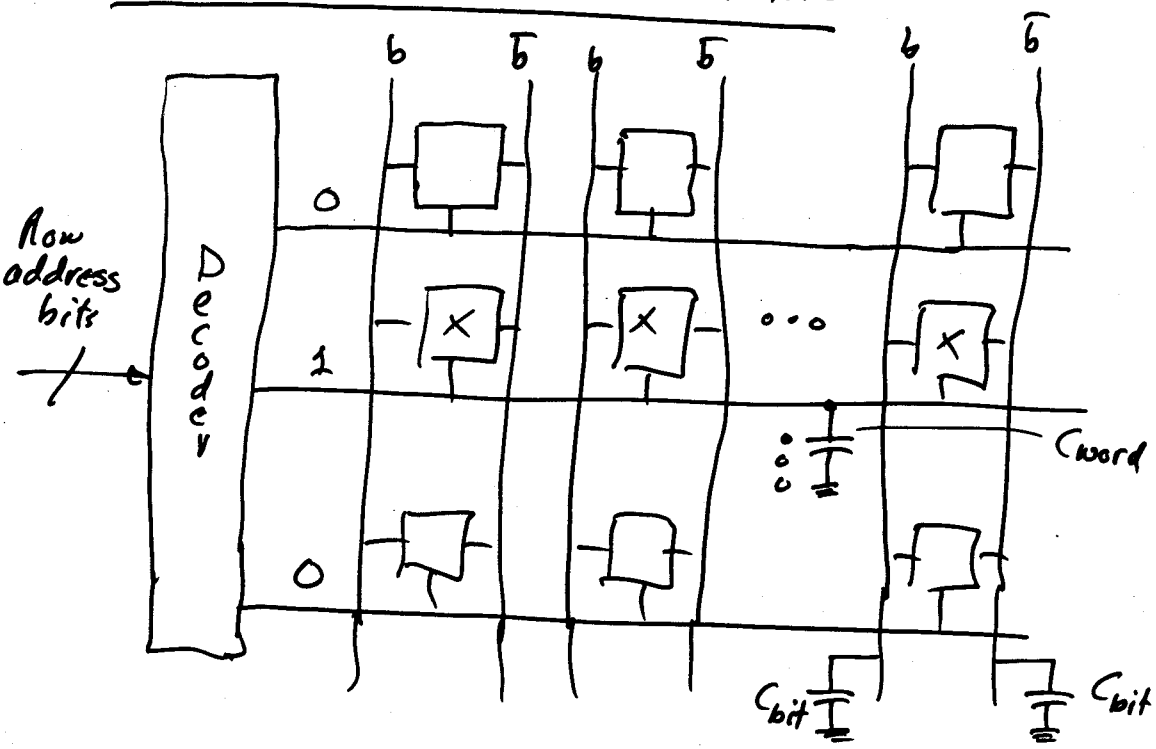




## 4 Transistor (4T)




$R \geq 10 M\Omega$

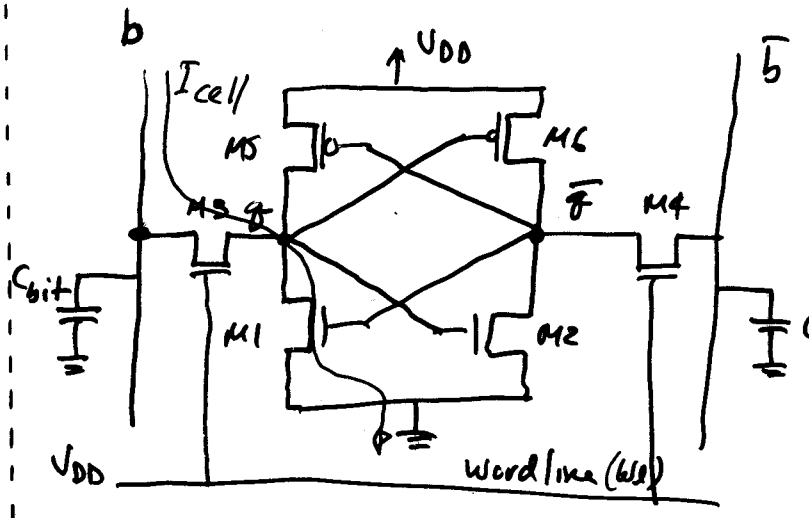
## Wordline and Double Bitline Architecture



$C_{word}$ = [(2 x gate capacitance) + wire capacitance] x no. of cells in a row

$C_{bit}$ = (Source/drain capacitance + wire capacitance) x no. of cells in a column

## Read Operation of the SRAM Cell




1.) Assume $q=0$ & $\bar{q}=1$

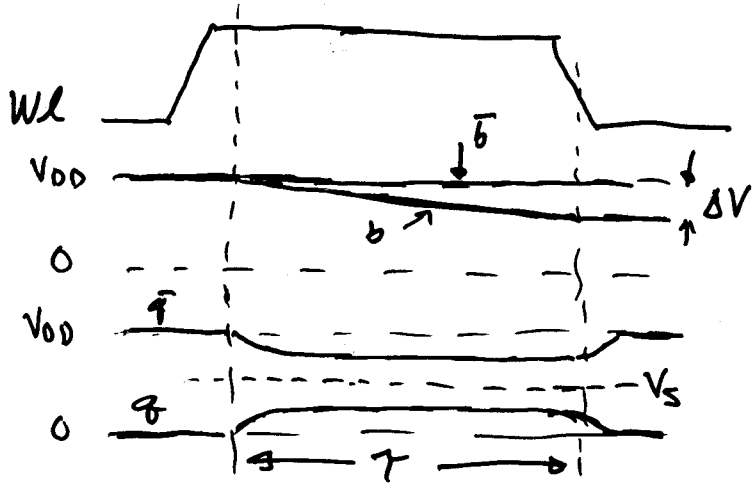
2.) Bit lines are precharged to $V_{DD}$

3.) M1 is ON and M2 off

4.) b drops, $\bar{b}$ stays at $V_{DD}$

5.) Difference between b and $\bar{b}$ is applied to the sense amplifier.

### Waveforms




$$I_{cell} = C_{bit}\frac{\Delta V}{\Delta T}$$

### Example 8.2 – Read Cycle Design Guideline

Compute $W_1$ and $W_3$ given that the q-node can change 0.1V during a read operation. Assume $C_{bit}$ = 2pF and that the sense amplifier requires a transition of 200mV on the bit line in 2ns. Use 0.13 μm technology.

$$I_{cell} = C_{bit} \times \frac{\Delta V}{\Delta T} = 2pF \times \frac{0.2V}{2ns} = 200\mu A$$