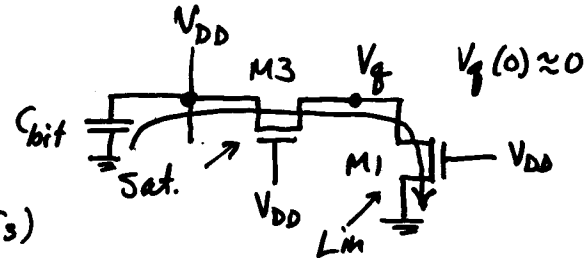
Example 8.2 – Read Cycle Design Guidelines

Compute W_1 and W_3 given that the q-node can change 0.1V during a read operation. Assume $C_{bit} = 2pF$ and that the sense amp. requires a 200mV transition of the bit line in 2ns. Use 0.13μm technology.



Solution

① $I_3 = I_1 \quad (I_1 = I_3)$

② $I_{cell} = C_{bit}\frac{\Delta V}{\Delta T} = 200\mu A$

$$\frac{W_1}{L_1}\frac{\mu_n C_{ox}}{\left(1+\frac{V_q}{E_{CN}L_1}\right)}\left[(V_{DD}-V_{T1})V_q - \frac{V_q^2}{2}\right] = \frac{W_3 N_{sat} C_{ox}\left(V_{DD}-V_q-V_{T3}\right)^2}{(V_{DD}-V_q-V_{T3}) + E_{CN}L_3}$$

$$\frac{W_1}{10^{-5}cm}\frac{270\ cm^2/V\cdot s}{\left(1+\frac{0.1}{0.6}\right)}\left[(1.2-0.4)(0.1)-\frac{0.1^2}{2}\right] = \frac{W_3\left(8\times10^6\frac{cm}{s}\right)(1.2-0.1-0.4)^2}{(1.2-0.1-0.4)+0.6}$$

1.6×10^{-6}

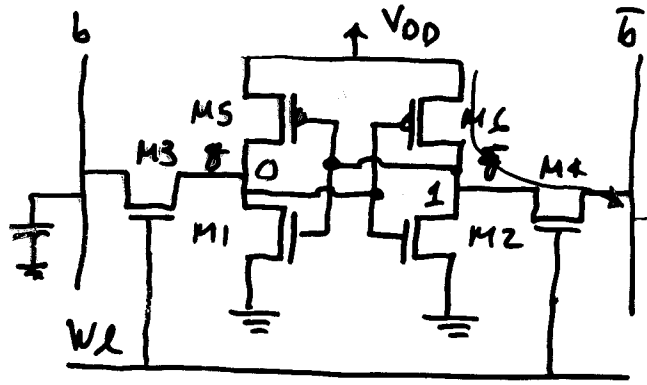
$$\frac{W_1}{W_3} = 1.73$$

$$I_{cell} = I_3 = \frac{W_3(2\times10^6)(1.6\times10^{-6})(1.2-0.1-0.4)^2}{1.3} \rightarrow W_3 = 0.4\mu m$$

$\therefore$ $W_1 \cong 1.7\,W_3 = 0.7\mu m$

Normal practice gives $\frac{W_1}{W_3} \approx 1.5$

Write Operation for a 6T SRAM Cell



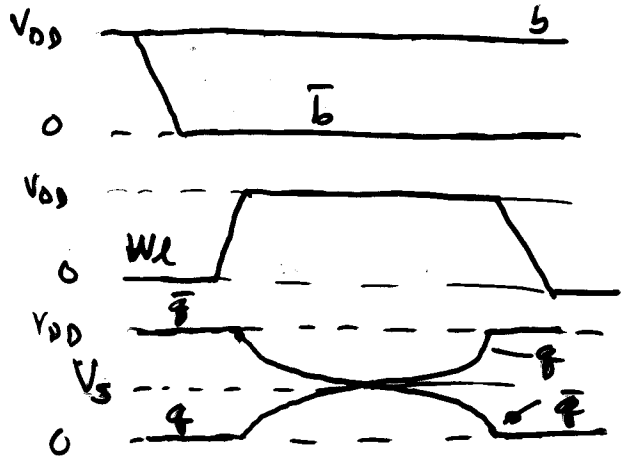
Operation to write a "1"

1.) $b = V_{DD}$ and $\bar{b} = 0$

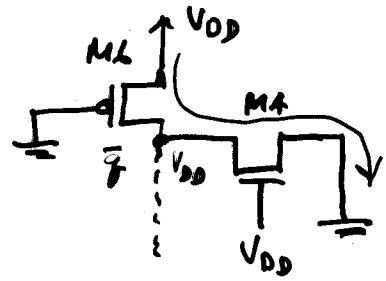
2.) When WL comes up, both M3 and M4 on

3.) Drain of M1 is pulled to V_{DD} and the drain of M2 is pulled to ground.

4.) When the drains of M1 and M2 pass V_S, regeneration occurs and completes the switching.



How do we size M6 and M4?



Typically $\frac{W_4}{W_6} \approx 1.5$

$$W_6 = \frac{W_4}{1.5} = \frac{W_3}{1.5} = \frac{W_1}{(1.5)^2} = \frac{W_1}{2.25} \rightarrow W_6 = \frac{W_1}{2.25}$$

6T SRAM Layout (See transparancy)

Ex. 8.3

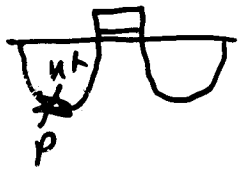
Find C_{word} and C_{bit} for the 64K RAM shown previously. Assume that $\frac{W_3}{L_3} = \frac{W_4}{L_4} = \frac{0.5\mu m}{0.1\mu m}$, the contacts on the bit lines are shared between pairs of cells and have a cap. of 0.5 fF each. Also assume wire capacitance is 0.2fF/μm and the cell layout is 40λ by 30λ (where 30λ = 1μm). Use 0.13μm technology.

Solution

$$C_{word} = \underbrace{256 \times (2C_g) \times W}_{C_g \text{ of M3 \& M4}} + \underbrace{256 \times \left(0.2\frac{fF}{\mu m}\right)(30\lambda)\left(\frac{1}{20}\frac{\mu m}{\lambda}\right)}_{\text{Bit line cap./cell}}$$

$$= 512fF + 77fF = 589fF$$

C_{bit} = S/D - Bulk capacitance + Contact Cap + Wire Cap of M3 and M4



Normally we would use C_{eff} (no rev. bias)
In this problem, assume $C_{eff} = 0.5fF$ because of a reverse bias of V_{DD}.

$$C_{bit} = (0.5fF/\mu m)256(0.5\mu m) + \frac{1}{2}256(0.5fF) + 256 \times 46\lambda\,(0.2fF/\mu m)\frac{1}{20}$$

$$= 64fF + 64fF + 102.4fF = 230fF$$

Contact capacitance?