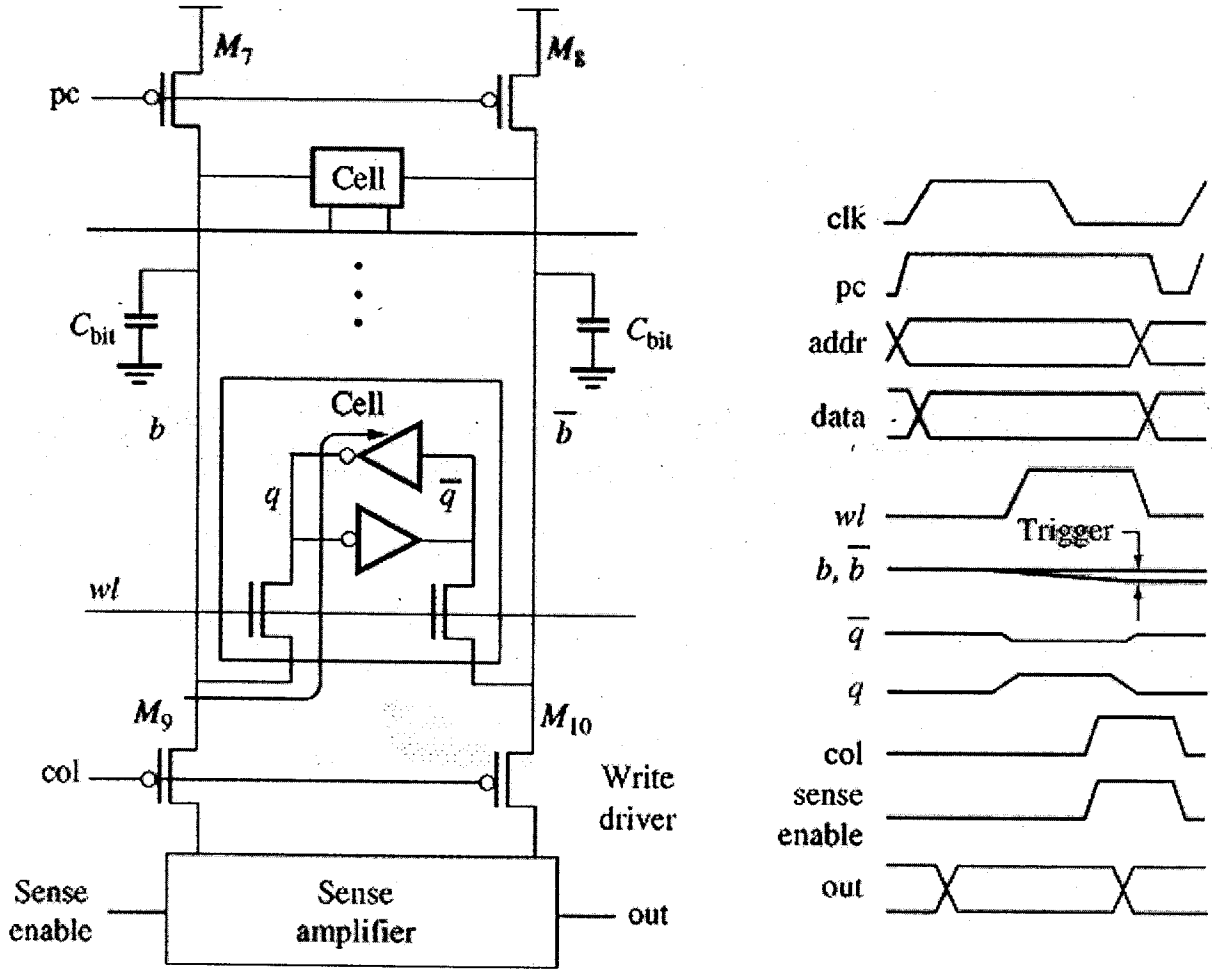
Read Circuitry

Figure 8.19 – Basic read circuit.

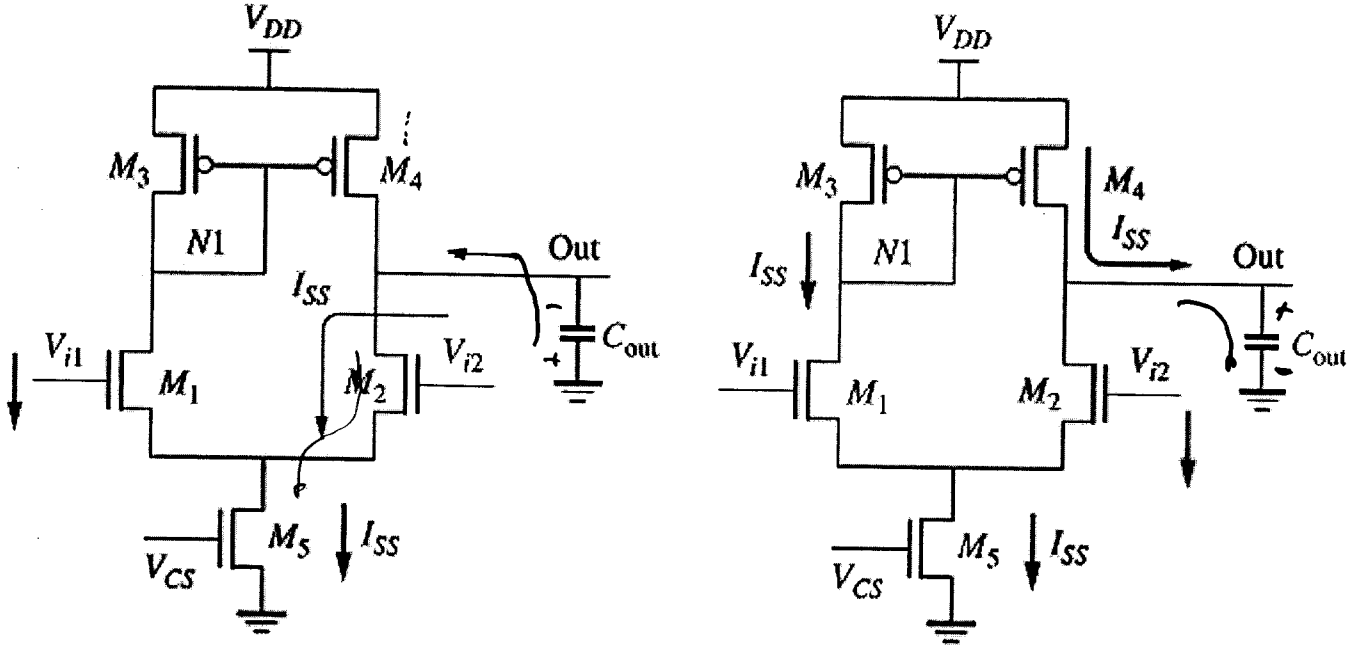


Operation

1.) Precharge circuits pull the column lines to V_{DD}
2.) The address, data and clock are applied
3.) The address signals translate into column enable and word line activation signals.
4.) The bitline with the initial 0 begins to fall
5.) Sense enable signal reads the difference and amplifies it.

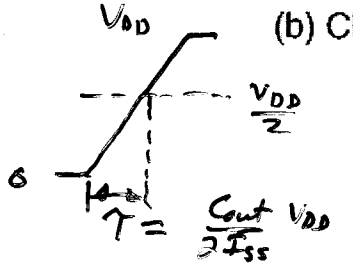
Sense Amplifiers

Figure 8.21 – Differential sense amplifier.



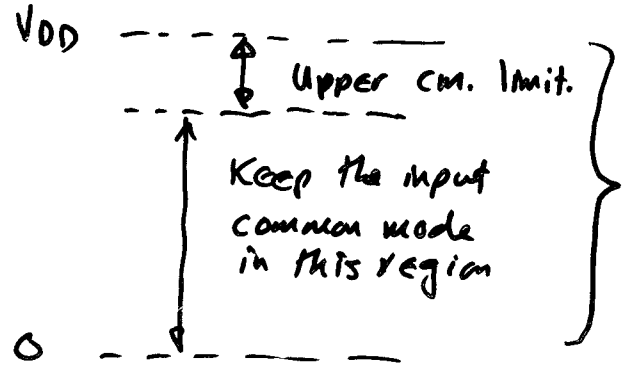
(a) Discharging output (b) Charging output

Max. $\frac{dV_{out}}{dt} = \frac{I_{SS}}{C_{out}}$



Maximum input common-mode range:

$V_{icm}^{+} = V_{DD} - V_{SGP} + V_{TN}$ ← The max. common mode voltage the sense amp. can have.

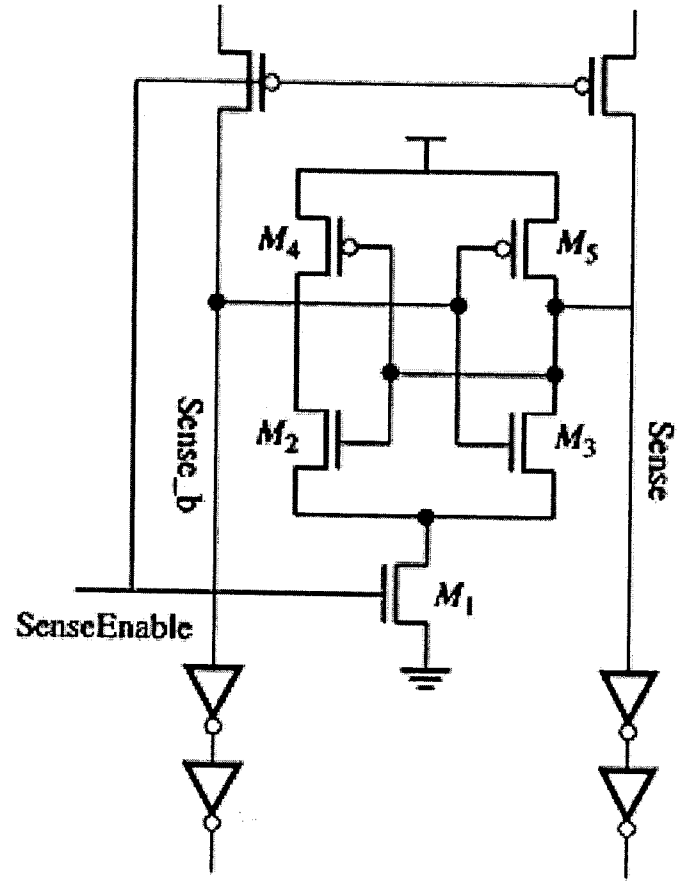


Makes Fig 8.13c much more attractive

$V_{bif}(max) = V_{DD} - V_T$

Assume $\Delta V = 0.1V$ if A_V (sense amp) = 50 → $V_{out} = 5V$!!!

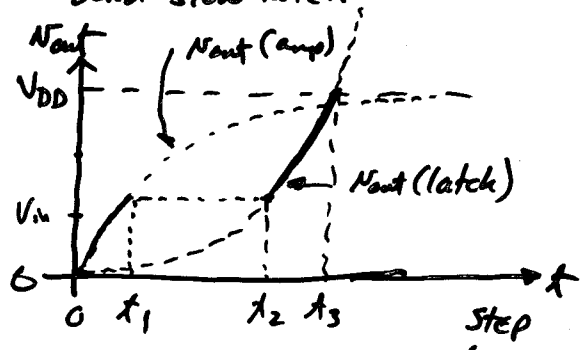
Figure 8.22 – Latch-based sense amplifier.



Positive fb. is slow initially and fast later.

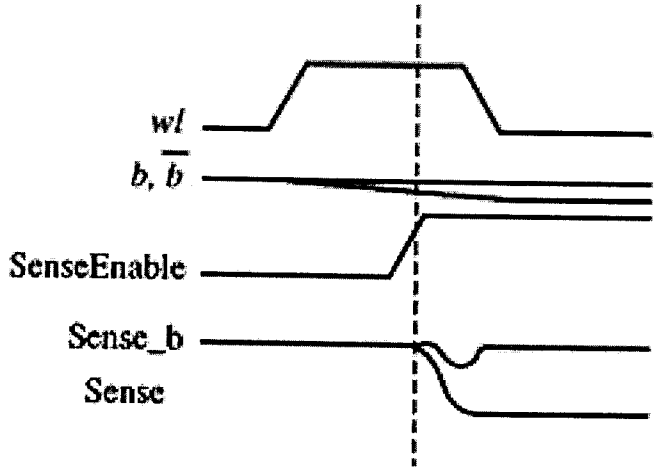
~~Negative~~

An amplifier is fast initially and slow later.



$V_{out}(latch) = K e^{t/\tau} V_{in}$

$V_{out}(amp) = K(1 - e^{-t/\tau}) V_{in}$

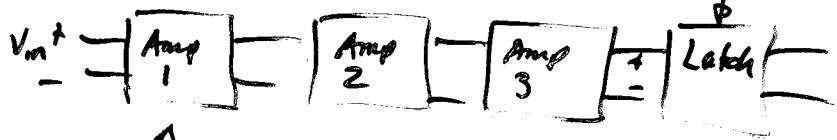


Fast sense amp:

Faster initially

Enable at t_1

Opt. results are 6 Amps with A = 3.16



$A_1(1 - e^{-t/\tau_1})$

Low power

Figure 8.23 – Replica circuit for sense amplifier clock enable

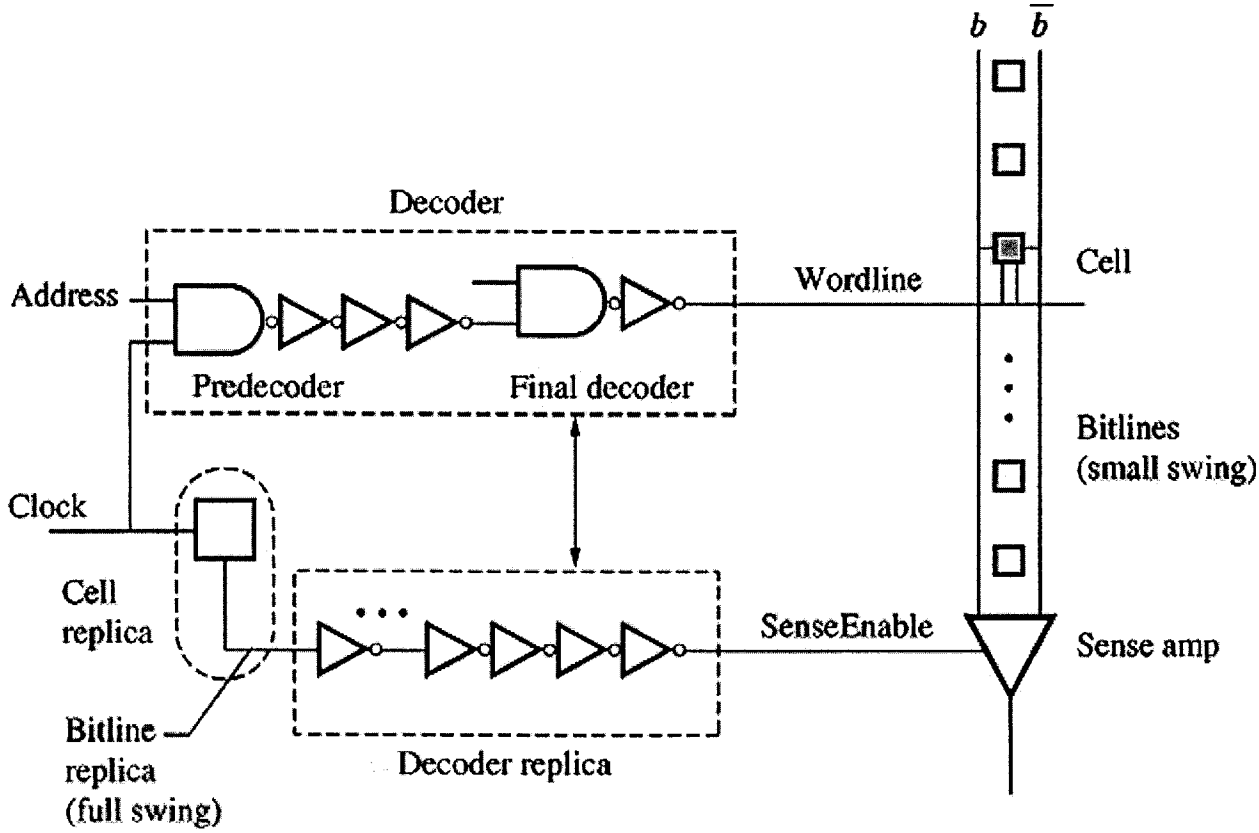
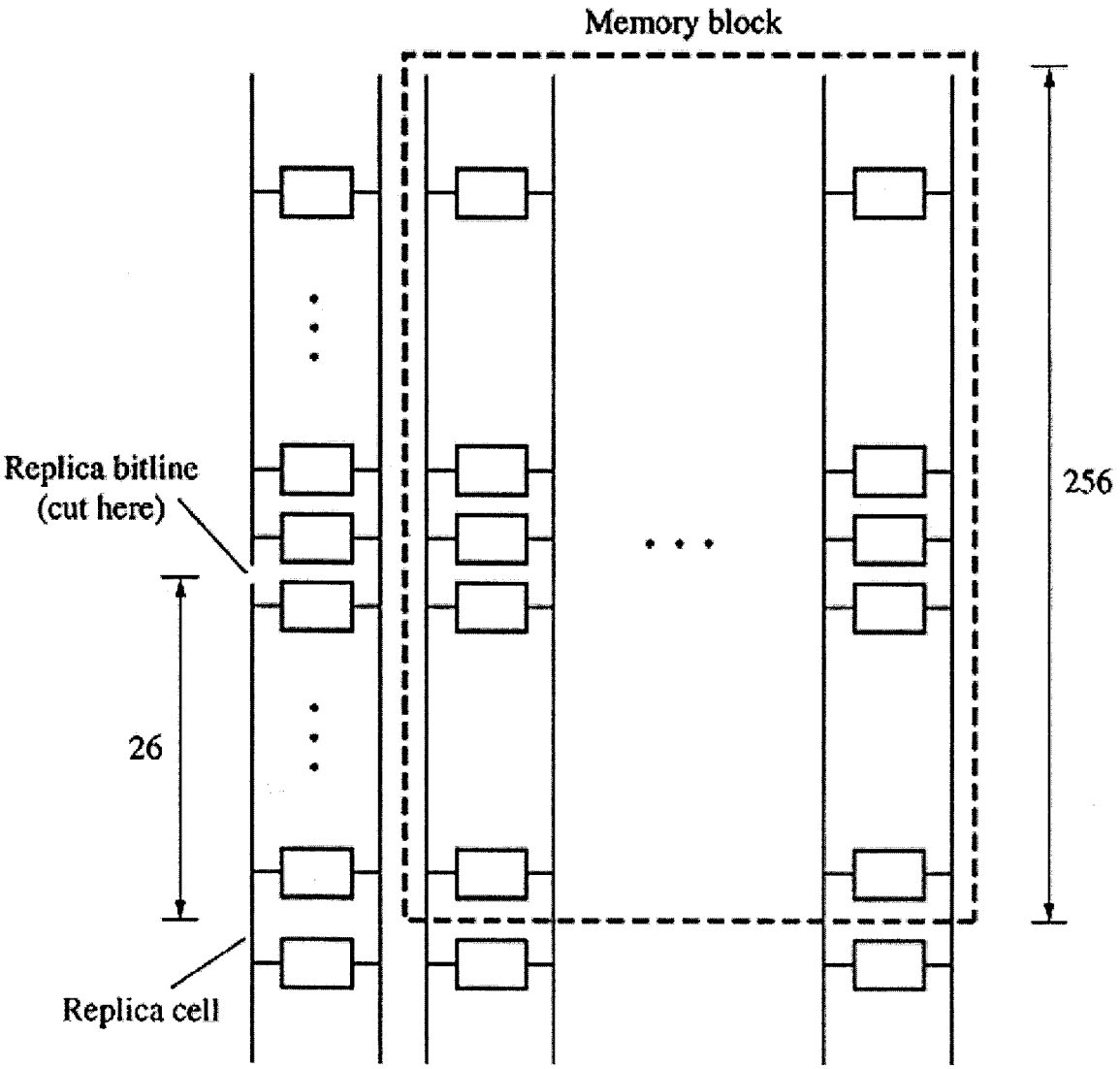


Figure 8.24 – Replica cell design.



Function of the replica cells is to achieve proper timing between the sense/enable signal and the cell output

- Single cell → Full swing is too slow (large C)
- Replica column like → ≈ 26 cells give the full swing with the desired delay.

Exam 3 ?

Chapt. 10 - Interconnects