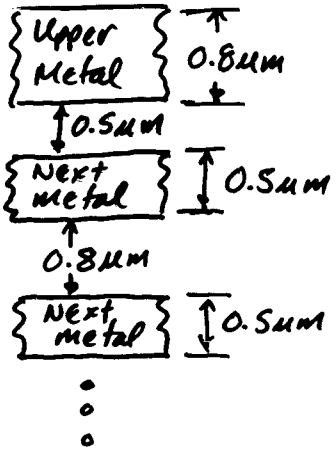
Final Exam – Tuesday, April 27, 8:00 – 10:50am

The final exam is optional if you are satisfied with your grade on the midterms and homework.

Lecture Continued on Interconnect Capacitance



For $W = 0.4\mu$,

	Closely Spaced $S = 0.4\mu m$	Widely Spaced $S = 4\mu m$
Upper Metal $T = 0.5\mu m$ $H = 0.5\mu m$	$C_{int} = 2C_A + 2C_L + 2C_F$ $= 2(0.03) + 2(0.07) + 0$ $\cong 0.2 fF/\mu m$	$C_{int} = 2C_A + 2C_F + 2C_L$ $= 2(0.03) + 2(0.025) + 0$ $\approx 0.1 fF/\mu m$
Lower Metal $T = 0.5\mu m$ $H = 0.8\mu m$	$C_{int} = 2C_A + 2C_L + 2C_F$ $= 2(0.015) + 2(0.035) + 0$ $\approx 0.1 fF/\mu m$	$C_{int} = 2C_A + 2C_F + 2C_L$ $\approx 2(0.015) + 2(0.025) + 0$ $\approx 0.1 fF/\mu m$

Support for the data in the table:

Upper metal –

$$C_A = 0.035\left(\frac{0.4}{0.5}\right) \approx 0.03 \qquad C_L = 0.035\left(\frac{0.8}{0.4}\right) = 0.07$$

$$C_F = 0.035 \ln\left(1 + \frac{0.8}{0.5}\right) = 0.033 \text{ ?}$$

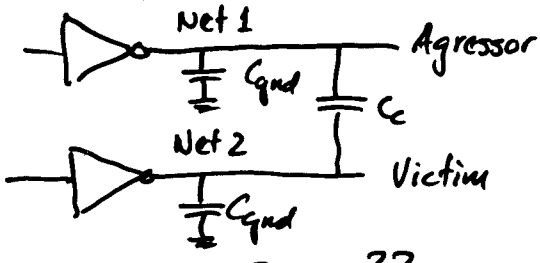
Lower metal –

$$C_A = 0.035\left(\frac{0.4}{0.8}\right) \approx 0.015 \qquad C_L = 0.035\left(\frac{0.5}{0.4}\right) \approx 0.035$$

$$C_F = 0.035 \ln\left(1 + \frac{0.5}{0.8}\right) = 0.014 \text{ ?}$$

Prob. Session Sunday 4pm5 7pm ??

Coupling Effects on Delay



Effective C_L of net 2	Condition
$C_{gnd} + C_c$	Agressor is not switching
C_{gnd}	Agressor is switching with the victim
$C_{gnd} + 2C$	Agressor is switching oppositely

Timing ??

Capacitive Noise or Crosstalk

Coupling from one net to another.

$$\Delta V_2 = \frac{C_c}{C_c + C_{gnd}} \Delta V_1$$

ΔV_1 = Voltage change on net 1

ΔV_2 = Resultant change on net 2 due to ΔV_1

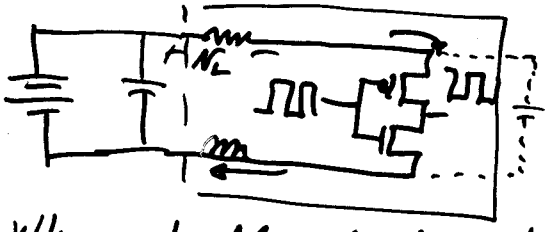
Interconnect Parasitics

Order of priority-

1.) Resistance

2.) Capacitance $i = C\frac{dv}{dt}$

3.) Inductance $V = L\frac{di}{dt}$ $\Rightarrow$ Fast current changes create voltage drops.



When should inductance be considered for wires?

1.) Lumped model

$$l_{max} < \frac{2}{R_{int}}\sqrt{\frac{L_{int}}{C_{int}}}$$

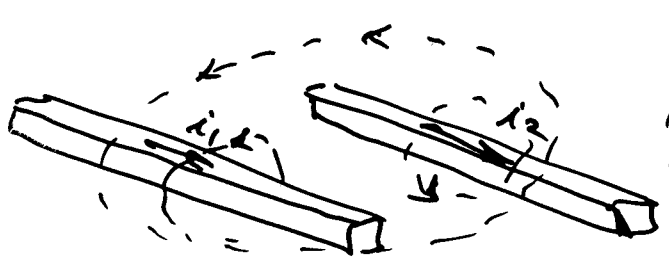
0.95pH/mm

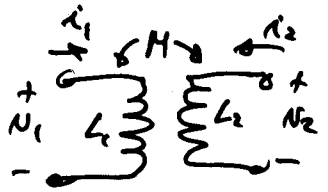
2.) Distributed model

$$l_{min} > \frac{t_r}{2\sqrt{L_{int}C_{int}}}$$

$$\frac{t_r}{2\sqrt{L_{int}C_{int}}} < l < \frac{2}{R_{int}}\sqrt{\frac{L_{int}}{C_{int}}}$$

Mutual inductance –





$$N_1 = L_1 \frac{di_1}{dt} + M \frac{di_2}{dt}$$

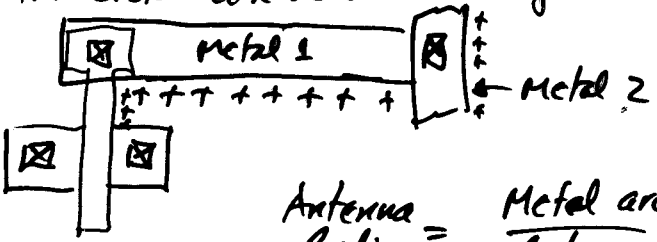
$$N_2 = M \frac{di_1}{dt} + L_2 \frac{di_2}{dt}$$

Transmission Lines

(see handout)

Antenna Effect

During fab, charge builds on each metal layer (charge is attached to metal like an antenna). If too much charge accumulates and the metal is connected to a gate, the transistor can become damaged.



$$\text{Antenna Ratio} = \frac{\text{Metal area}}{\text{Gate area}}$$

1.) Antenna diode – reverse biased pn junction which removes the charge

2.) Break long wires with a buffer insertion.

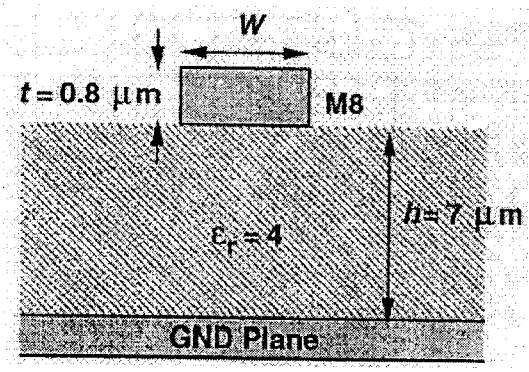
3.) Metal jumpers

Illustration of Transmission Lines in Modern IC Technology[†]

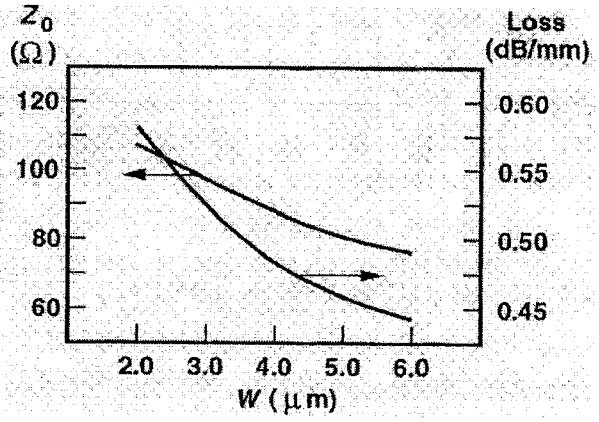
With the availability of multiple layers of metal, CMOS technology can implement transmissions lines with reasonable loss and small capacitance per unit length.

• Performance of microstrip structure.

CMOS microstrip structure:

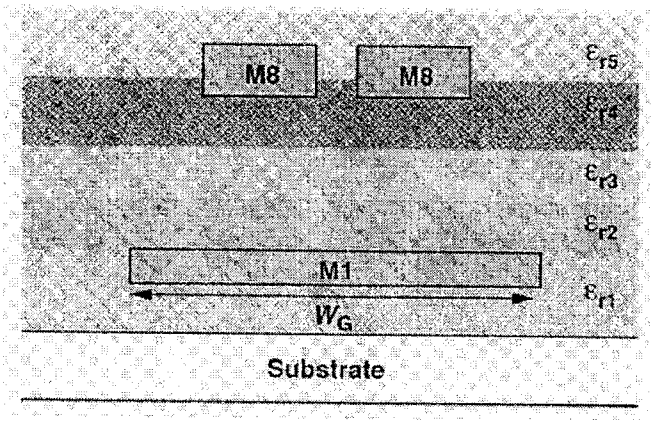


Loss and characteristic impedance:



• Differential transmission lines are possible and have given reasonable results.

A practical differential transmission line structure:



A transmission line in 0.35μm CMOS:

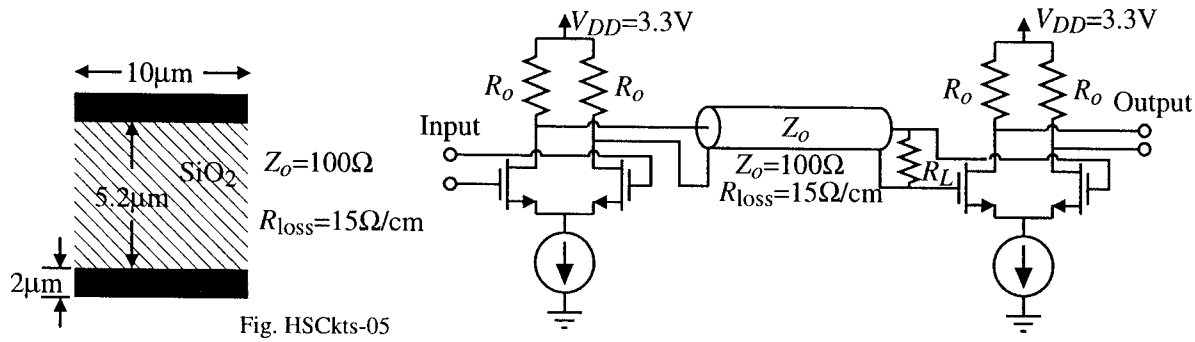


Fig. HSCkts-05

[†] B. Razavi, "The Role of Monolithic Transmission Lines in High-Speed Integrated Circuits," *IEEE 2002 Custom Integrated Circuit Conf.*, pp. 367-373.