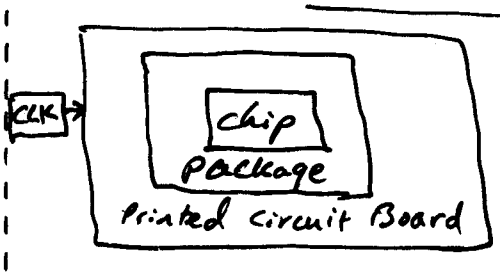
CHAPTER 11 - POWER GRID AND CLOCK DESIGN

DEAL WITH HOW TO DISTRIBUTE VDD, GND, AND CLK TO VARIOUS POINTS ON THE CHIP

POWER DISTRIBUTION DESIGN



Problems:

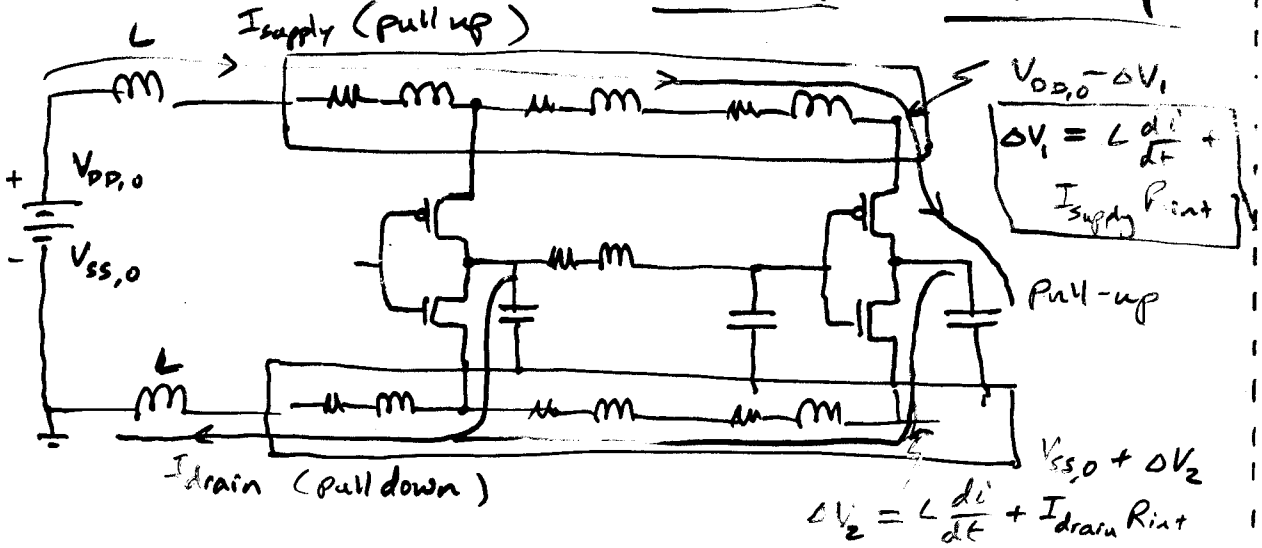
1) CLK frequency ↑
2) Current ↑
3) Power ↑
4) # of Transistors ↑

According to 2003 ITRS (public.itrs.net)

	nd #	Vdd	CLK	AMP
Year 2004	90 nm	1.2 V	~4 GHz	158 Watts
Year 2018	18 nm	0.7 V	~53 GHz	300 Watts

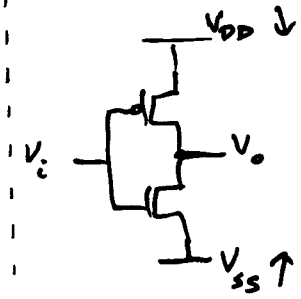
Al → Cu ⇒ R ↓ } ⇒ Rc delay → LC delay
0.18 um 0.13 um CLK ↑

Illustration of IR drop & $L\frac{di}{dt}$ drop



Worst case : Far end of Line node
& Simultaneous Switching

To see the effects of IR drop and $L\frac{di}{dt}$ drop let's revisit the inverter (ref. Fig. 4.12 P.168)



First observation:

IR and $L\frac{di}{dt}$ drop cause

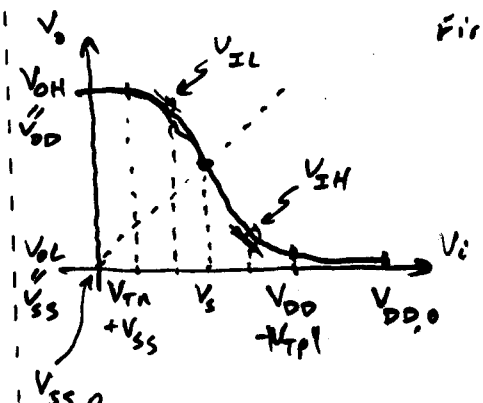
V_{DD} ↓ and V_{SS} ↑

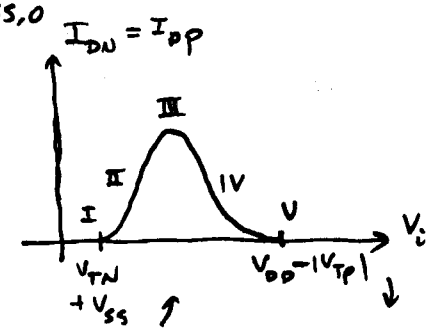
So what?

First response: Power ↓ OK.

$$\begin{cases} NM_H = V_{OH}\downarrow - V_{IH}\uparrow \quad \downarrow\downarrow \\ NM_L = V_{IL}\downarrow - V_{OL}\uparrow \quad \downarrow\downarrow \end{cases}$$

Reliability worse!





If $V_{DD}-|V_{TP}|$ ↓

$V_{TN}+V_{SS}$ ↑

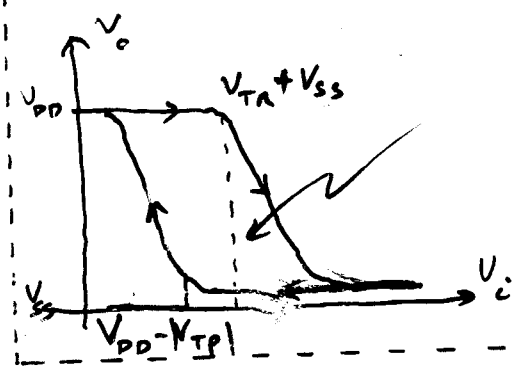
then we see III will disappear.

i.e. no region where both nmos and pmos in sat. ⇒ gain ↓

⇒ Regeneration ↓ (Noise)

Roughly, $V_{DD}-V_{SS} \geq 2V_T = 2\frac{KT}{q} \cong 50$ mV to sustain a gain > 1

Yet, another interesting thing will happen:



HYSTERISIS!

i.e. V_i has no control over V_o!

When $V_{TN}+V_{SS} > V_{DD}-|V_{TP}|$

i.e. $V_{DD}-V_{SS} \leq V_{TN}+|V_{TP}|$

Electromigration:

At high current levels, metal molecules will migrate and can result in SHORT or OPEN circuits.

Measuring metric: Mean-time-to-failure = MTTF

$$MTTF = \frac{A}{J^2} \exp\left(\frac{\Delta H}{KT}\right) \quad \propto \quad \frac{1}{J^2}$$

where $J = \frac{I_{avg}}{W \cdot T}$ = average dc current density

Power Supply Routing:

1) $\uparrow$ IR drop $\quad R = \frac{\rho}{T}\frac{L}{W}$

To reduce

no control vertically
have control horizontally
$\Rightarrow \downarrow L \quad \uparrow W$

use Cu instead of Al $\Rightarrow \downarrow \rho$
and less aggressively scale down T

2) $\uparrow L\frac{di}{dt}$

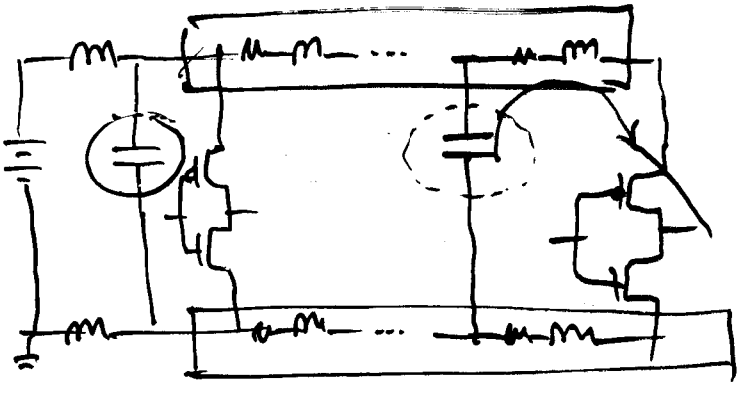
To reduce

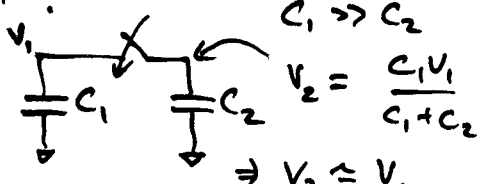
Keep Line short

don't run Lines in parallel w/ current in the same direction (mutual Ind.)

Decoupling Capacitance Design

BIG Capacitance to ground helps to hold the interconnect potentials constant.





$C_1 \gg C_2$

$V_2 = \frac{C_1 V_1}{C_1 + C_2}$

$\Rightarrow V_2 \cong V_1$

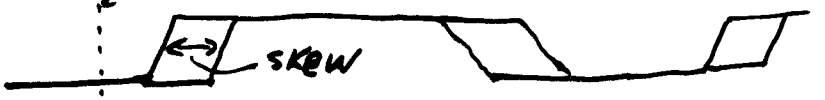
CLOCK AND TIMING ISSUES

Clock Definitions and metrics:

Ideal clock:

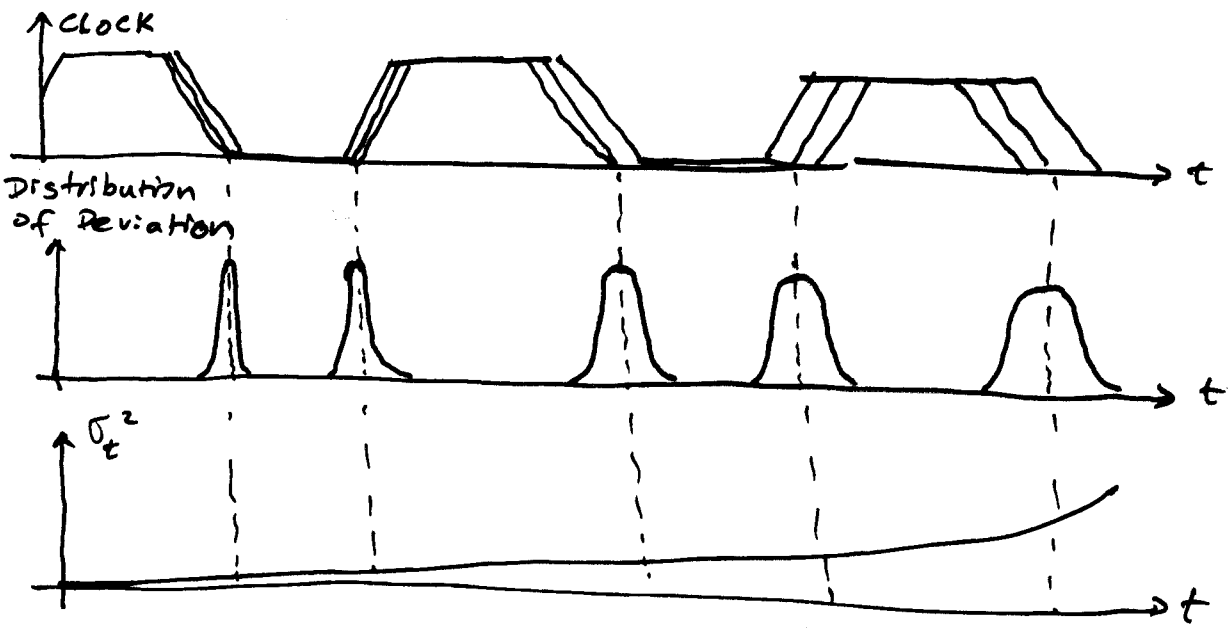
Clock with finite rise time and delay
Fall time (latency)

Clock with finite rise/Fall time, latency and skew (SAME CLOCK at DIFFERENT Locations)



edge

Clock jitter (time domain, at SAME POINT)



σ_t^2 = variance

Accumulative effect of the timing uncertainty

Short-time jitter: $\sigma_t \propto \sqrt{t}$

Long-time jitter: $\sigma_t \propto t$