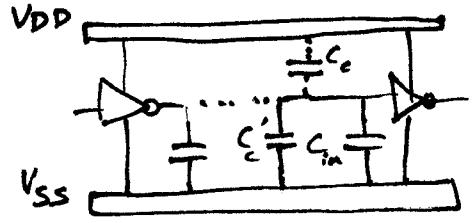
CLK ≡ heartbeats of digital systems

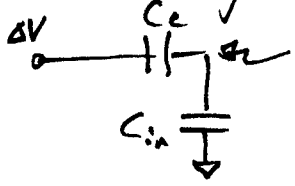
Ideally, CLK should have: minimum rise / fall times
specified duty cycles
zero skew etc

How noise come in ?



Due to switching activities and IR drop & $L\frac{di}{dt}$ drop along the power supply (V_{DD}) and GND (V_{ss}) Lines/Buses.

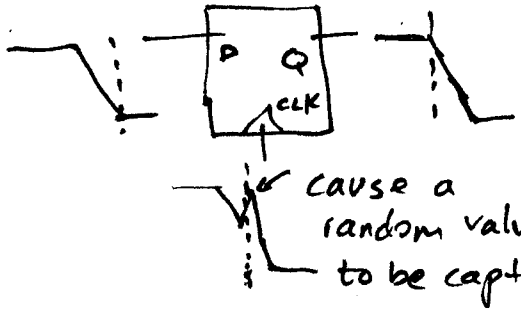
the voltage along VDD. Vss changes. They're not stay const. at 1.8 V or 0 V for 0.18 um e.g.



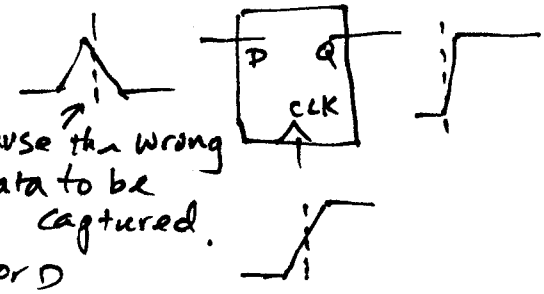
$\frac{C_c}{C_c+C_{in}}\Delta V$ ⇒ Affects the reliability

Effect of Noise on clk and FFs.

Glitch on clk input:



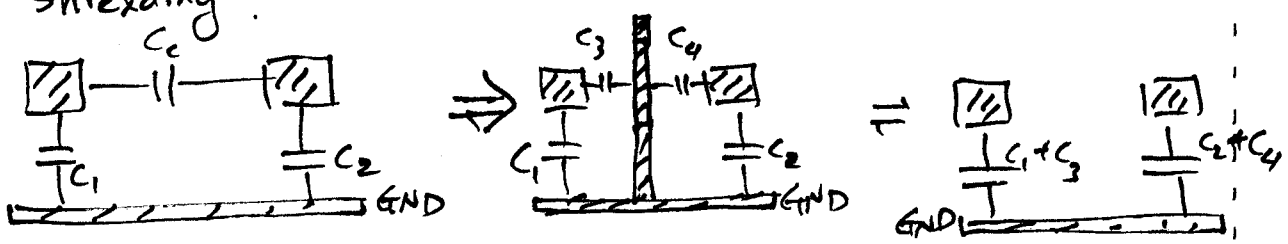
Glitch on data input:



solution to ~~reduce~~ noise:

① $C = \varepsilon\frac{A}{d}$ ⇒ ↑ d Not area efficient!

② shielding

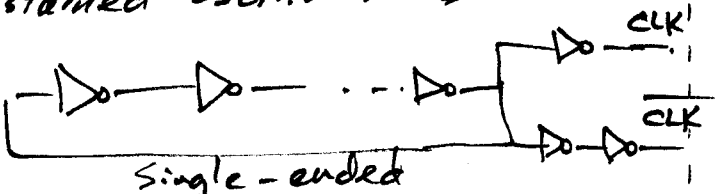


How to generate CLK ?

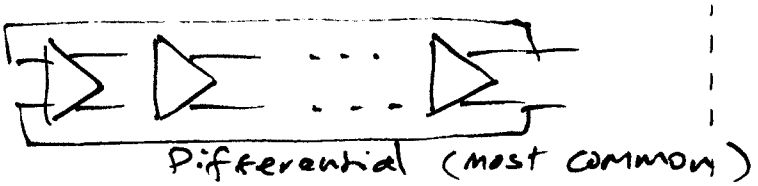
need some sustained Oscillation ⇒ + feedback

Consider CLK as some sustained Oscillation ⇒ + feedback

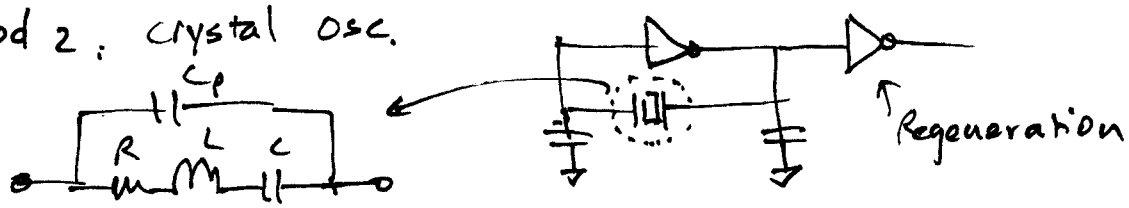
Method 1. Ring Osc.



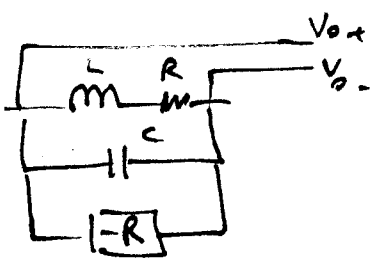
To reject the VDD, GND noise use :



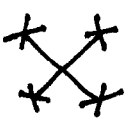
Method 2. crystal Osc.



Method 3. LC Osc.



CLK Distribution (uniformly over chip. minimize CLK skew.)



Vertical crossing → minimize mutual ind.

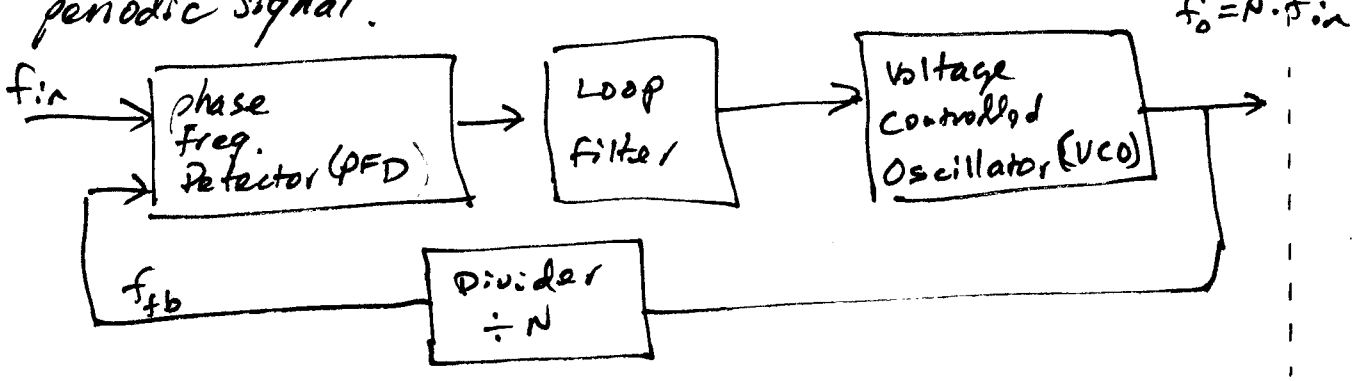
CLK Stabilization (minimize the jitter)

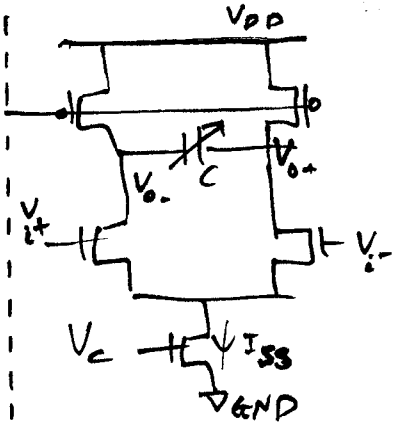
via

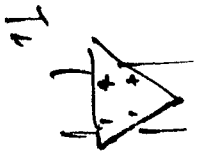
Phase - Locked Loop (PLL) technique.

PLL design Considerations :

The function of the PLL is to generate a periodic signal whose frequency is related to an input or reference periodic signal.







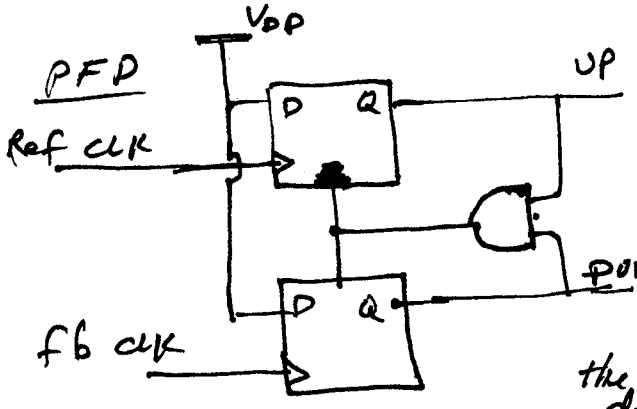
$$f_{osc} \approx \frac{1}{2Nt_d}$$

$$C\frac{\Delta V}{\Delta t} = I_{ss} \Rightarrow t_d \simeq C\frac{\frac{V_{DD}}{2}}{I_{ss}}$$

Control ~~tab~~ Knobs :

① C

② $I_{ss} \rightarrow V_c$

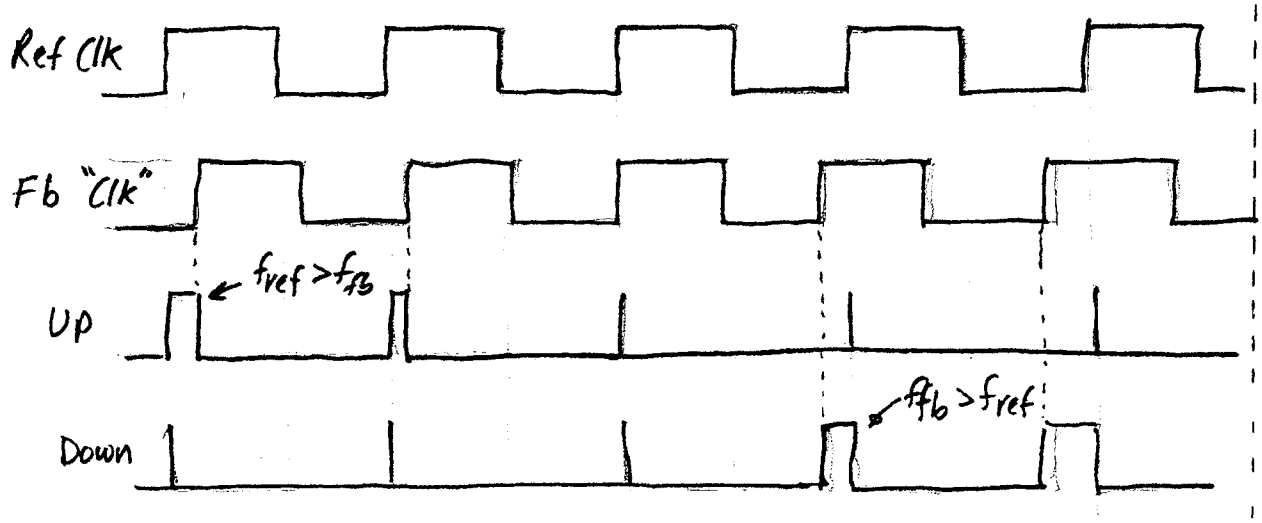


Operation :

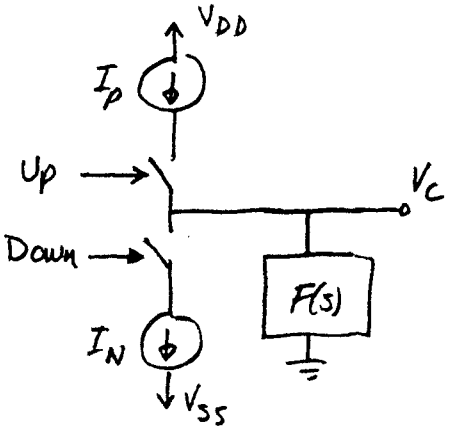
1) If rise edge of Ref CLK precede rising edge of fb CLK, UP = 1 during the difference

2) If rising edge of Ref. CLK follows the rising edge of fb CLK, Down = 1 during the difference

Example –



Charge Pump and Loop Filter



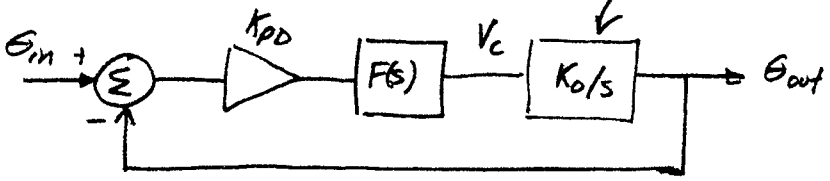
The charge pump combines with the continuous time filter to implement the loop filter of the PLL. F(s) generally contains capacitors and resistors.

$f_{out} = K_0 V_c$

$\theta_{out} = \int f_{out}\, dt = K_0 \int V_c(t)\, dt$

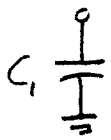
$\theta_{out}(s) = \frac{K_0 V_c(s)}{s}$

System Block Diagram



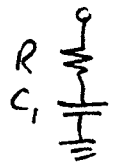
$$\therefore \theta_{out} = (\theta_{in} - \theta_{out})\left[K_{PD} F(s) \frac{K_0}{s}\right] \rightarrow \frac{\theta_{out}(s)}{\theta_{in}(s)} = \frac{K_{PD} F(s) \frac{K_0}{s}}{1 + K_{PD} F(s) \frac{K_0}{s}} = \frac{G(s)}{1+G(s)}$$

F(s)



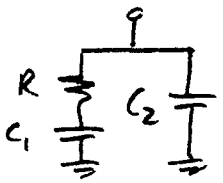
$G(s) = \frac{K_0 K_{PD}}{s^2}$

Unstable



$G(s) = K_{PD}\left(\frac{RC_1 s + 1}{s}\right)\frac{K_0}{s}$

Stable



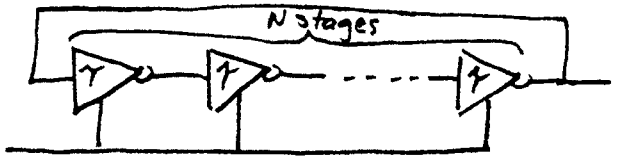
$$G(s) = \left(\frac{b-1}{b}\right)\left(\frac{s\tau_1 + 1}{sC_1\left(\frac{s\tau_1}{b} + 1\right)}\right)\frac{K_0}{s}$$

$b = 1 + \frac{C_1}{C_2}$ and $\tau_1 = RC_1$

Stable

Example of a 3rd-order PLL with a charge pump (see handout)

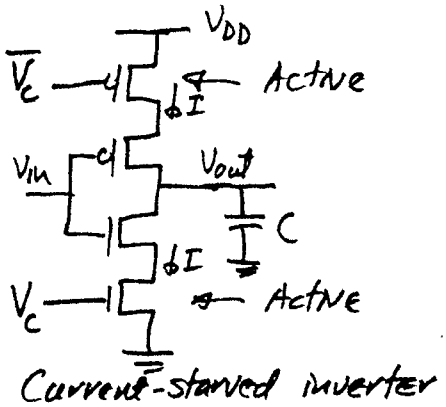
VCO



$f = \frac{1}{2N\tau}$

$i = C\frac{dV}{dt} \rightarrow I = C\frac{\Delta V}{\tau} \rightarrow \tau = \frac{C\Delta V}{I} = \frac{C V_{DD}}{2I}$

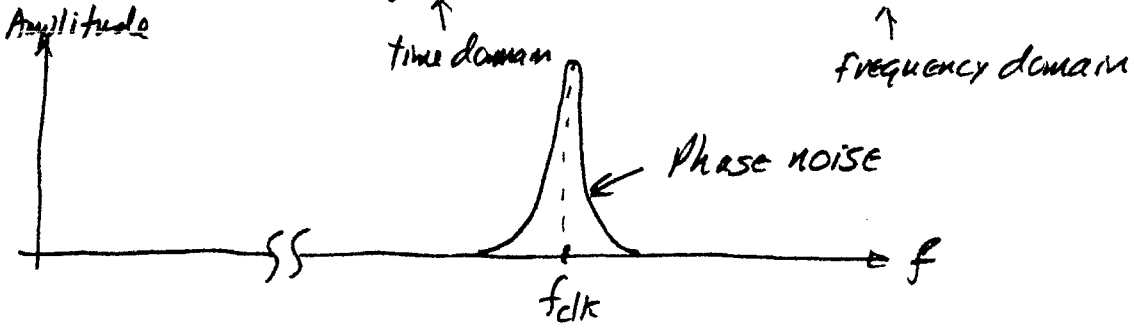
$I = K(V_c - V_T)^{\alpha}$



Current-starved inverter

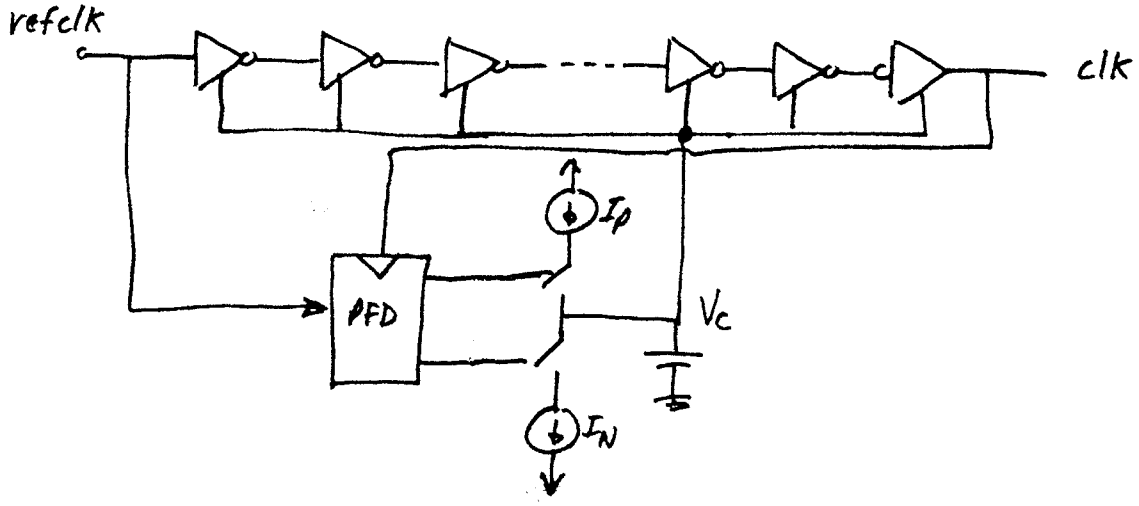
Performance Issues of the PLL

- f_{ref} can be a crystal and is very stable ($f_{out} = N f_{ref}$)
- If f_{out} is large (GHz), the divider can be power hungry
- The VCO is subject to jitter which causes phase noise



Delay Locked Loop (Data synchronization – CDR circuits)

Implementation:



- Simple
- Transfers jitter to the output

Clock Distribution Considerations

(See handout)