COURSE DETAILS AND INFORMATION FOR ECE4420 – Digital Integrated Circuits

Instructors: Dr. Phillip E. Allen, Room 292B, Van Leer, 894-6251 (office), pallen@ece.gatech.edu

Lecture: Monday, Wednesday, and Friday, 12:05am to 12:55am, Room C240, Van Leer

Office Hours: Allen: 10-11 MF and 11-12pm W or by e-mail <pallen@ece.gatech.edu>.

Prerequisite: EE 3040 Microelectronic Circuits or permission of instructor.

Text:

Analysis and Design of Digital Integrated Circuits – Third Edition, David A. Hodges, Horace G. Jackson and Resve A. Saleh, McGraw-Hill, 2003.

Electronic Copies of Class Handouts: You may download pdf copies of all classroom material at the following web site: http://users.ece.gatech.edu/~pallen/Academic/

Objectives: The purpose of this course is to enable the student to model, analyze and design digital integrated circuits using primarily MOS technologies. At the conclusion of the course, the student should be able to successfully perform the electrical and physical design of digital circuit in an industrial environment.

Examinations: There will be three, closed book midterm examinations each of 50 minute duration and a 3 hour final examination. The final examination will be given during the regularly scheduled time for the final exam. All grades become final one week after they are returned in class.

Final Exam: The final exam is on Thursday, May 5, 2005, from 8am to 10:50am.

Homework: Homework will be assigned and will be graded.

Course Grading Policy: Your grade will be determined using the following scheme:

Three midterm exams……..	60%
Homework……	10%
Final Exam……	30%

Grades will be assigned on a curve and will not necessarily be consistent with 100>A>90, 90>B>80, etc..

Computer Usage: You are expected to be able to use HSPICE or PSPICE for classroom assignments. Most assignments using the computer will work on the student version of PSPICE. The educational version of PSpice for the PC is free and downloadable from:

http://www.orcad.com/products/pspice/eval_f.htm
http://www.electronics-lab.com/downloads/schematic/013/

Attendance: You are responsible for all course materials, announcements, notes, etc. made during our regular class meeting times. Prompt arrival to class is appreciated.

Academic Honesty: It is the responsibility of the instructor to encourage an environment where you can learn and your accomplishments will be rewarded fairly. Any behavior that compromises the basic rules of academic honesty as described in the General Catalog will not be tolerated.

Classroom Behavior: Smoking, drinking and eating is prohibited in the classroom by Institute rules.

Weekly Coverage of Topics for ECE4420

Week	Lecture	Date	Topic	Text (pages)
1	1	1/10	Review of Digital Logic Gate Design	6-15
	2	1/12	Digital Integrated Circuit Design	15-24
	3	*1/14*	MOS Transistor	35-45
	4	1/17	Holiday	-
	5	*1/19*	Large Signal MOS Model	45-57
	6	*1/21*	Short Channel Technology	57-68
3	-	1/24	Subthreshold Operation and MOS Capacitances	68-80
	7	1/26	IC Fabrication Technology	89-96
	8	1/28	IC Fabrication Technology – Continued	96-107
4	9	1/31	SPICE MOS Model	107-115
	10	2/2	Additional effects in MOS Transistors	125-130
	11	*2/4*	MOS Inverters	143-153
5	12	2/7	Resistive Load Inverter Design	153-161
	13	2/9	Active Load Inverters	162-178
	-	2/11	Examination No. 1	-
6	14	2/14	Psuedo MOS Inverters, Sizing, Tristate	178-185
	15	2/16	CMOS Gate Inverters	195-209
	16	2/18	Complex CMOS Gates	209-214
7	17	*2/21*	Complex CMOS Gates/Flip-Flops	209-227
	18	*2/23*	Flip Flops	214-227
	19	*2/25*	Power Dissipation in CMOS Gates	227-240
8	20	2/28	Power Dissipation in CMOS Gates	227-240
	21	3/2	Switching Time Analysis /Load Capacitance Calculation	249-267
	22	*3/4*	Switching Time Analysis /Load Capacitance Calculation	249-267
9	23	3/7	Improving Delay	267-276
	24	3/9	Improving Delay /Gate Sizing for Optimal Delay	257-276
	-	3/11	Examination No. 2	-
10	25	3/14	Improving Delay /Gate Sizing for Optimal Delay	257-276
	26	3/16	Gate Sizing for Optimal Delay	276-300
	27	3/18	Transfer Gates	309-318
		3/21-3/25	Spring Break	
11	28	3/28	CMOS Transmission Gate Logic	318-333
	29	3/30	Dynamic D-Latches and D-Flip Flops/ Domino Logic	333-340
	30	4/1	Domino Logic	340-349
12	31	4/4	MOS Decoders	359-368
	32	4/6	Static RAM Cell Design	368-377
	33	*4/8*	SRAM Column I/O Circuitry	377-390
13	34	4/11	Interconnects	441-453
	35	4/13	Buffers, Interconnect Coupling Capacitance	453-468
	36	4/15	Inductance, Antenna	469-476
14	37	4/18	Power Distribution	483-499
	38	4/20	Clock and Timing Issues	499-514
	-	4/22	Examination No. 3	
15	39	4/25	PLLs and DLLs	514-524
	40	4/27	BJTs	547-558
	41	4/29	BJT Logic	558-562
			Final Exam is Thursday, May 5, 2005 from 8:00-10:50am	