REVIEW FOR EXAMINATON 1

Examination No. 1 will be given during class on Friday, February 11, 2005 from 12:05pm to 12:55pm. It will last for 50 minutes and is closed book.   The exam will contain all model information and formulas that you will need for the exam.   The exam will consist of 3-4 problem. Below is a list of the material for which you are responsible.

Deep Submicron Digital IC Design

Review of Digital Logic Gate Design
Basic logic functions
     - DeMorgan's Laws
     - Sequential Logic Circuits
Implementation of Logic Circuits
     - Characteristics
Noise Margins
Propagation Delay Time
Power
     - Static
     - Dynamic

MOS Transistors

Structure and operation of MOSFETs
     - Equivalent ON and OFF resistances
Threshold voltage of the MOSFET
     - Equation (2.11) – its components and their meaning and the parameters of Eq. (2.11)
Development and application of the First-Order (Sah model) Current-Voltage
     Characteristics
Development and application of the Velocity-Saturated Current-Voltage Model
Application and understanding of the Subthreshold Conduction Model
Capactances of the MOSFET
     - Thin-oxide (intrinsic capacitances)
     - PN-junction capacitances (depletion capacitances)
     - Overlap capacitances (intrinsic capacitances)
The summary in Sec. 2.9 is key to this section – you must know these formulas, what they
     mean and how to apply them.

Fabrication, Layout and Simulation

IC Fabrication Technology
     - What are the five major processing steps in IC technology? Also you should know
       about the epitaxial process
     - Photolithography process – what is it and how is it applied
     - Know the physical aspects of the MOSFET – cross-section
     - Connections – metal, vias, etc.
Calculation of capacitance and resistance of a conductor
Calculating the resistance and capacitance associated with the physical layout of a MOSFET
Circuit simulation models for the MOSFET
     SPICE – Level 1 model and parameters
Extraction of the level 1 model parameters
Temperature dependence of MOSFETs for the various regions of operation
Voltage limitations
Latchup

MOS Inverter Circuits

Voltage transfer characteristic – V_{OH}, V_{OL}, V_{IH}, V_{IL}, V_S
Noise Margins (Multiple source noise margin)
Resistive load inverter design - V_{OH}, V_{OL}, V_{IH}, V_{IL}, V_S