EXAMINATION NO. 1 - SOLUTION

(Average Score = 79.1/100)

Problem 1 - (25 points)

A logic circuit is modeled as shown. Assume that at time $t = 0$, the capacitor is uncharged and the switch is connected to the "high" state. At some time later, after the output voltage has reached its high state, the switch is connected to the "low" state. Find the propagation time delay of this logic circuit.

S05E1P1
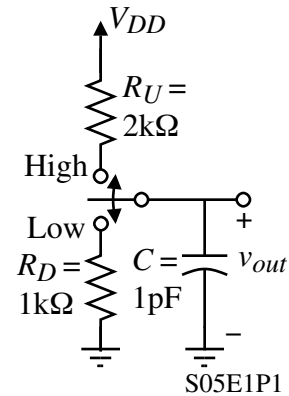
Solution

Risetime:

The model for this case is,
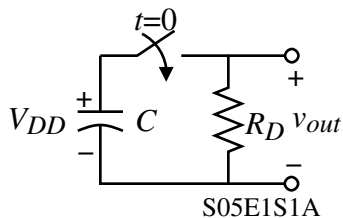

S05E1S1
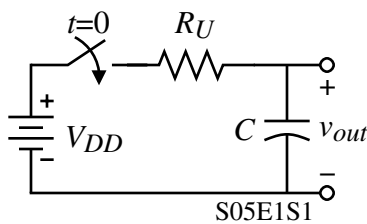
An expression for the output voltage is,

$$v_{out} = V_{DD}(1 - e^{-t/\tau_1})$$

where $\tau_1 = R_U C = 2\text{ns}$

When $v_{out} = 0.5V_{DD}$, then $t = T_1$.

$\therefore$ $0.5 = 1 - e^{-T_1/\tau_1}$ $\rightarrow$ $T_1 = \tau_1 \ln(2) = 0.693(2\text{ns}) = 1.386\text{ns}$

Falltime:

The model for this case is,

S05E1S1A

An expression for the output voltage is,

$$v_{out} = V_{DD}\, e^{-t/\tau_2}$$

where $\tau_2 = R_D C = 1\text{ns}$
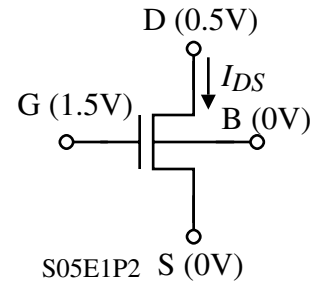
When $v_{out} = 0.5V_{DD}$, then $t = T_2$.

$\therefore$ $0.5 = e^{-T_1/\tau_1}$ $\rightarrow$ $T_2 = \tau_2 \ln(2) = 0.693(1\text{ns}) = 0.693\text{ns}$

The propagation delay time, T_d, is found as:

$$T_d = \frac{T_1 + T_2}{2} = \frac{1.386 + 0.693}{2} = \underline{\underline{1.04\text{ns}}}$$

Problem 2 – (25 points)

Solve for the dc value of the drain current, I_{DS}, for the NMOS transistor shown assuming 0.18μm CMOS technology. The W and L for this transistor are given in Problem 3.

G (1.5V) D (0.5V)

B (0V)

I_{DS}

S05E1P2 S (0V)

Solution

Check for saturation.

$$V_{DS}(\text{sat}) = \frac{(V_{GS} - V_T)E_cL}{(V_{GS} - V_T) + E_cL} = \frac{(1.5\text{-}0.5)(1.2)}{(1.5\text{-}0.5) + 1.2} = 0.5454\text{V}$$

$V_{DS} = 0.5\text{V} \Rightarrow$ NMOS in linear region

$$\therefore I_{DS} = \frac{W}{L} \frac{\mu_e C_{ox}}{\left(1 + \frac{v_{DS}}{E_cL}\right)} \left(V_{GS} - V_T - \frac{V_{DS}}{2}\right) V_{DS}$$

$$= \frac{0.6}{0.2} \frac{(270 \text{ cm}^2/\text{V·s})(1\mu\text{F}/\text{ cm}^2)}{1 + \frac{0.5}{1.2}} (1.5\text{-}0.5\text{-}0.25)(0.5) = 3\frac{270 \cdot 1}{1.416} (0.75)(0.5)\mu\text{A}$$

$$= \underline{\underline{214\mu\text{A}}}$$

Problem 3 – (25 points)

Given the layout for the NMOS transistor of Problem 2, find the value of C_{gs}, C_{gd}, C_{gb}, C_{db}, and C_{sb} assuming that the junction depth of the source-drain diffusions is $x_j = 50$ nm, $m = 0.5$ and the lateral diffusion is 10nm.

100nm

Shallow
Trench
Isolation

Source

Poly Gate

Drain

S04E1P3

100nm
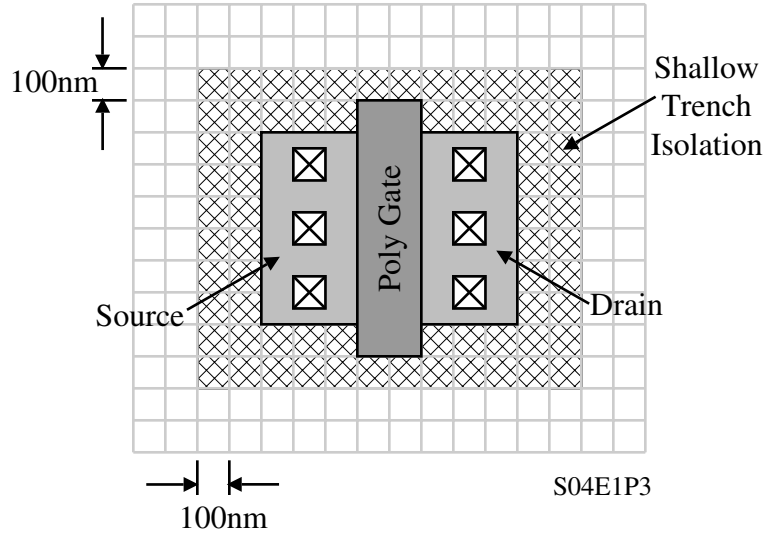
Solution

From Problem 2, we know that the NMOS transistor is in the linear region. To make the calculations, we will need C_g and C_{ov}. They are calculated as follows,

$$C_g = C_{ox} \cdot W \cdot L = 1 \times 10^{-6} \ (\text{F/cm}^2) \cdot 0.6 \times 10^{-4} (\text{cm}) \cdot 0.2 \times 10^{-4} (\text{cm}) = 1.212 \times 10^{-15} \text{ F}$$

$$C_{ol} = C_{ox} \cdot LD = 1 \times 10^{-6} \ (\text{F/cm2}) \cdot 10 \times 10^{-7} (\text{cm}) = 1 \times 10^{-12} \text{ F/cm}$$

$$\therefore \ C_{gs} = C_{ol} \cdot W + 0.5 C_g = (1.01 \times 10^{-12})(0.6 \times 10^{-4}) + (0.5)(1.212) = (0.061 + 0.606) \text{fF}$$
$$= \underline{\underline{0.666 \text{ fF}}}$$

$$C_{gd} = C_{ol} \cdot W + 0.5 C_g = (1.01 \times 10^{-12})(0.6 \times 10^{-4}) + (0.5)(1.212) = (0.061 + 0.606) \text{fF}$$
$$= \underline{\underline{0.666 \text{ fF}}}$$

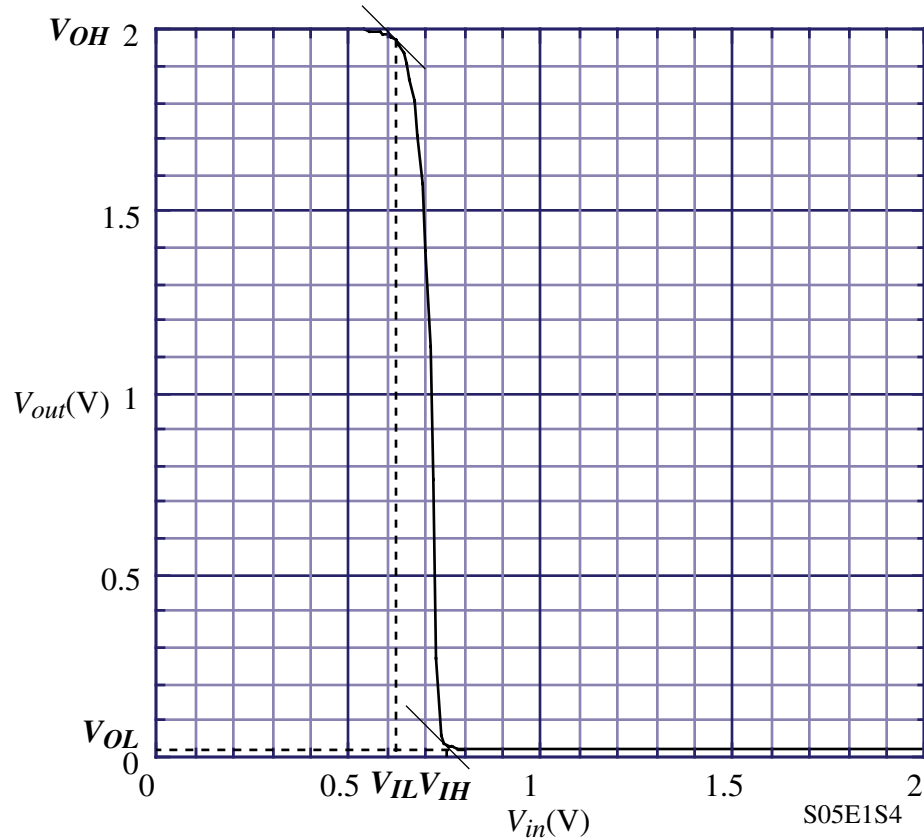$$C_{gb} = \underline{\underline{0}}$$

$$C_J = \frac{C_{jb} \ (A_b + A_{sw})}{\left(1 - \dfrac{V_j}{\phi_B}\right)} = \frac{C_{j0} \ (A_b + A_{sw})}{\left(1 - \dfrac{V_j}{\phi_B}\right)}$$

$$C_{bd} = \frac{1.6 \text{fF}/\mu\text{m}^2 [(0.3)(0.6) + (0.05)(0.6)]}{\sqrt{1 + \dfrac{0.5}{0.9}}} = \underline{\underline{0.269 \text{ fF}}}$$

$$C_{bs} = \frac{1.6 \text{fF}/\mu\text{m}^2 [(0.3)(0.6) + (0.05)(0.6)]}{\sqrt{1 + 0}} = \underline{\underline{0.336 \text{ fF}}}$$

Problem 4 – (25 points)

The transfer function curve for an inverter is shown. Find the values of V_{OH}, V_{OL}, V_{IL}, and V_{IH} from the curve below. Use this information to find the values of NM_H and NM_L.

From the curve we get the following numerical values.

$V_{OH} = \underline{\underline{2.0}}$, $V_{OL} = \underline{\underline{0.02V}}$, $V_{IL} = \underline{\underline{0.62V}}$, and $V_{IH} = \underline{\underline{0.75V}}$

The noise margins are,

$$NM_H = V_{OH} - V_{IH} = 2.0 - 0.75 = \underline{\underline{1.25V}}$$

and

$$NM_H = V_{IL} - V_{OL} = 0.62 - 0.02 = \underline{\underline{0.60V}}$$