

**EXAMINATION NO. 1**

NAME \_\_\_\_\_ SCORE \_\_\_\_\_ /100

**INSTRUCTIONS:** This exam is closed book. You are allowed to have one page of handwritten (or typed) notes (both sides). The exam consists of 4 questions for a total of 100 points. Please show your work leading to your answers so that maximum partial credit may be given where appropriate. Be sure to turn in your exam with the problems in numerical order, firmly attached together.

**TRANSISTOR INFORMATION:**

The following is for an NMOS transistor only (with appropriate sign changes they can be used for PMOS transistors):

$$V_T = V_{T0} + \gamma(\sqrt{|2\phi_F| + V_{SB}} - \sqrt{|2\phi_F|})$$

For long-channel devices, the current equations are:

$$\text{If } V_{GS} \geq V_T$$

$$\text{and } V_{DS} \geq V_{GS} - V_T \text{ (the saturation region)} \quad I_{DS} = \frac{k}{2} (V_{GS} - V_T)^2 (1 + \lambda V_{DS})$$

$$\text{or } V_{DS} \leq V_{GS} - V_T \text{ (the linear region)} \quad I_{DS} = \frac{k}{2} [2(V_{GS} - V_T)V_{DS} - V_{DS}^2]$$

$$\text{If } V_{GS} < V_T \text{ (subthreshold region)} \quad I_{DS} \approx 0$$

For velocity saturated short-channel devices, the current equations are:

$$\text{If } V_{GS} \geq V_T$$

$$\text{and } V_{DS} \geq \frac{(V_{GS} - V_T)E_c L}{(V_{GS} - V_T) + E_c L} \text{ (saturation region)} \quad I_{DS} = W v_{sat} C_{ox} \frac{(V_{GS} - V_T)^2}{(V_{GS} - V_T) + E_c L}$$

$$\text{or } V_{DS} < \frac{(V_{GS} - V_T)E_c L}{(V_{GS} - V_T) + E_c L} \text{ (linear region)} \quad I_{DS} = \frac{W}{L} \frac{\mu_e C_{ox}}{\left(1 + \frac{V_{DS}}{E_c L}\right)} \left(V_{GS} - V_T - \frac{V_{DS}}{2}\right) V_{DS}$$

$$\text{If } V_{GS} < V_T \text{ (subthreshold region)} \quad I_{DS} = I_s \exp\left(\frac{q(V_{GS} - V_T - V_{offset})}{nkT}\right) \left[1 - \exp\left(\frac{-qV_{DS}}{kT}\right)\right]$$

Name	Symbol	0.18μm		0.13μm		Units
		NMOS	PMOS	NMOS	PMOS	
Oxide Thickness	$t_{ox}$	35	35	22	22	Å
Oxide Capacitance	$C_{ox}$	1.0	1.0	1.6	1.6	μF/cm <sup>2</sup>
Threshold Voltage	$V_{T0}$	0.5	-0.5	0.4	-0.4	V
Body-Effect Term	$\gamma$	0.3	0.3	0.2	0.2	√ <sup>0.5</sup>
Fermi Potential	$2 \phi_F $	0.84	0.84	0.88	0.88	V
Junction Cap. Coeff.	$C_{j0}$	1.6	1.6	1.6	1.6	fF/μm <sup>2</sup>
Built-In Junct. Potential	$\phi_B$	0.9	0.9	1.0	1.0	V
Grading Coefficient	$m$	0.5	0.5	0.5	0.5	-
Nominal Mobility	$\mu_o$	540	180	540	180	cm <sup>2</sup> /V·s
Effective Mobility	$\mu_e$	270	70	270	70	cm <sup>2</sup> /V·s
Critical Field	$E_c$	6x10 <sup>4</sup>	24x10 <sup>4</sup>	6x10 <sup>4</sup>	24x10 <sup>4</sup>	V/cm
Critical Field x L	$E_c L$	1.2	4.8	0.6	2.4	V
Effective Resistance	$R_{eff}$	12.5	30	12.5	30	kΩ/sq.

## CAPACITOR INFORMATION:

	Cutoff	Linear	Saturation
$C_{gs}$	$C_{ol}$	$C_{ol} + 0.5C_g$	$C_{ol} + 0.67C_g$
$C_{gd}$	$C_{ol}$	$C_{ol} + 0.5C_g$	$C_{ol}$
$C_{gb}$	$1/(1/C_g+1/C_{jc}) < C_{gb} < C_g$	0	0
$C_{sb}$	$C_{jSB}$	$C_{jSB} + \alpha_1 C_{jc}$	$C_{jSB} + \beta_1 C_{jc}$ ( $\alpha, \beta$ small)
$C_{db}$	$C_{jDB}$	$C_{jDB} + \alpha_2 C_{jc}$	$C_{jDB} + \beta_2 C_{jc}$ ( $\alpha, \beta$ small)

where,  $C_{ol}$  = overlap capacitance     $C_{jc}$  = channel to substrate depletion capacitance

$$C_g = C_{ox} L$$

$$C_j = \frac{C_{jb}(A_b + A_{sw})}{\left(1 - \frac{V_j}{\phi_B}\right)^{mj}}$$

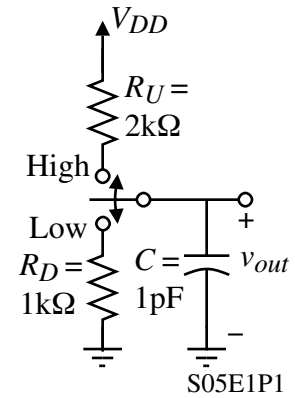
where  $A_b$  = area of source/drain and  $A_{sw}$  = area of side of source/drain facing the channel

## OTHER INFORMATION:

$$\varepsilon_{ox} = 4\varepsilon_o = 4 \cdot 8.85 \times 10^{-14} \text{ F/cm} = 3.54 \times 10^{-13} \text{ F/cm}$$

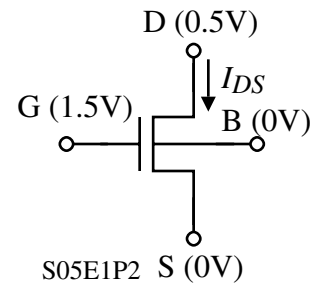
**Problem 1 - (25 points)**

A logic circuit is modeled as shown. Assume that at time  $t=0$ , the capacitor is uncharged and the switch is connected to the “high” state. At some time later, after the output voltage has reached its high state, the switch is connected to the “low” state. Find the propagation time delay of this logic circuit.



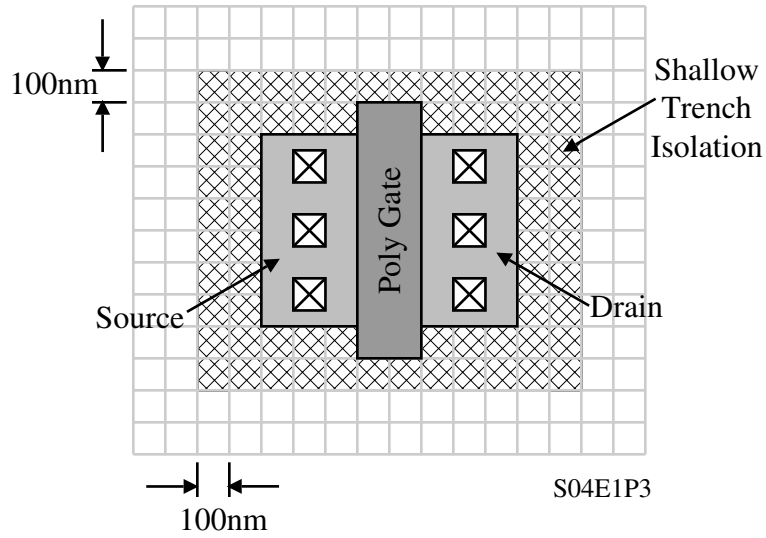
**Problem 2 – (25 points)**

Solve for the dc value of the drain current,  $I_{DS}$ , for the NMOS transistor shown assuming  $0.18\mu\text{m}$  CMOS technology. The  $W$  and  $L$  for this transistor are given in Problem 3.



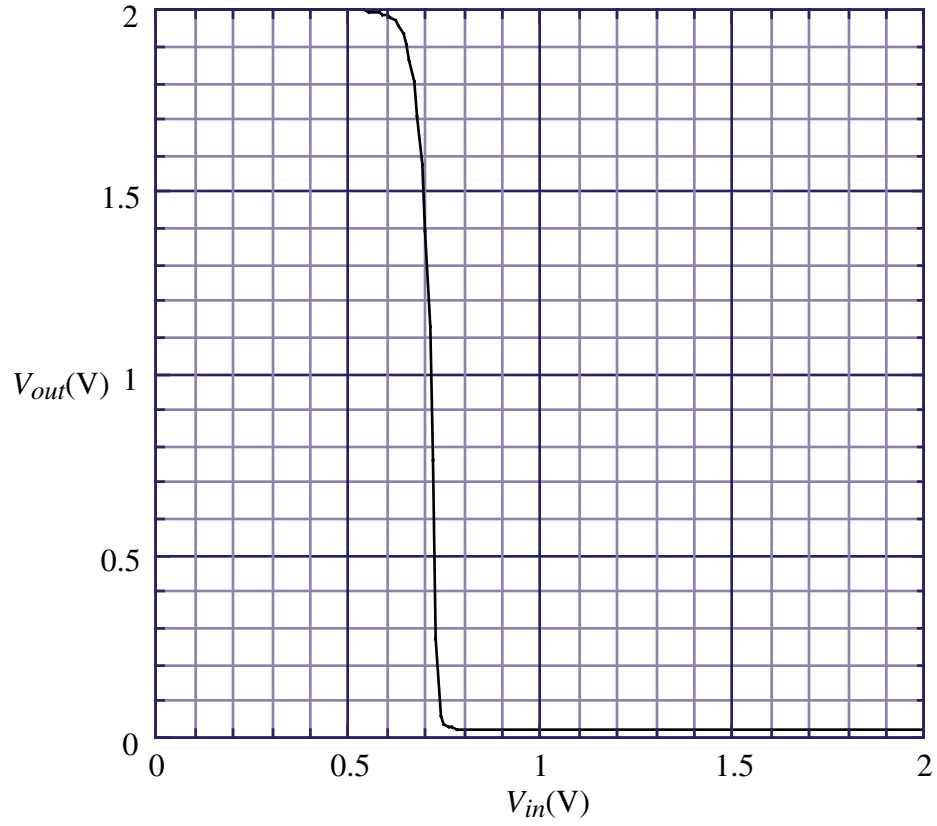
**Problem 3 – (25 points)**

Given the layout for the NMOS transistor of Problem 2, find the value of  $C_{gs}$ ,  $C_{gd}$ ,  $C_{gb}$ ,  $C_{db}$ , and  $C_{sb}$  assuming that the junction depth of the source-drain diffusions is  $x_j = 50$  nm,  $m = 0.5$  and the lateral diffusion is 10nm.



**Problem 4 – (25 points)**

The transfer function curve for an inverter is shown. Find the values of  $V_{OH}$ ,  $V_{OL}$ ,  $V_{IL}$ , and  $V_{IH}$  from the curve below. Use this information to find the values of  $NM_H$  and  $NM_L$ .



Extra Sheet