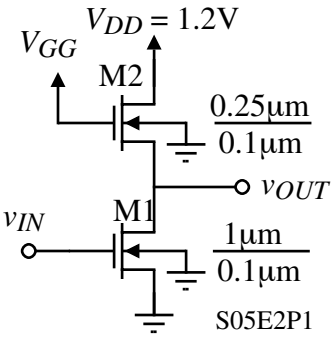
EXAMINATION NO. 2 - SOLUTIONS

(Average score = 77/100)

Problem 1 - (25 points)

The inverter shown is to be designed in a 0.13μm technology to have V_{OH} = 1.2V and V_{OL} = 0.1V. (a.) Find the value of V_{GG} needed to produce the desired value of V_{OH}. (b.) What is the region of operation for each transistor when the input is at V_{DD} and the output is at V_{OL} (use the value of V_{GG} found above)? (c.) How much current flows in each transistor when the input is at V_{DD} and the output is low? (The current in each transistor does not have to be equal.)



Solution

(a.) V_{OH} occurs when v_{IN} = 0 which means the NMOS is off. Assuming no current flow in M1 or M2, then V_{OH} would be equal to $V_{GG} - V_{TN}$.

Assuming that $v_{OUT} \approx V_{OH}$ = 1.2V allows us to find $|V_{TP}|$ as,

$$V_{TN} = V_{TN0} + \gamma\sqrt{2\phi_F + V_{BS}} - \gamma\sqrt{2\phi_F} = 0.4 + 0.2\sqrt{0.88+1.2} - \sqrt{0.88} = 0.5\text{V}$$

$$\therefore V_{GG} = V_{TN} + V_{DD} = \underline{1.7\text{V}} \qquad (5)$$

(b.) Ignore bulk effects since both drains are close to ground. Find V_{DS}(sat) for both transistors.

M1: V_{GS} = 1.2V $\rightarrow$ $V_{DS1}(\text{sat}) = \dfrac{(V_{GS}-V_{TN})E_C L}{V_{GS}-V_{TN}+E_C L} = \dfrac{0.8(0.6)}{0.8+0.6} = 0.343\text{V}$

$V_{DS1} = V_{OL} < V_{DS}(\text{sat}) \Rightarrow$ <u>M1 is linear/active</u> (5)

M2: $V_{GS} = V_{GG} - V_{OL} = 1.6\text{V} \rightarrow V_{DS2}(\text{sat}) = \dfrac{(V_{GS}-V_{TN})E_C L}{V_{GS}-V_{TN}+E_C L} = \dfrac{1.2(0.6)}{1.2+0.6} = 0.4\text{V}$

$V_{DS2} = 1.2\text{-}0.1 = 1.1\text{V} > V_{DS2}(\text{sat}) \Rightarrow$ <u>M2 is saturated</u> (5)

(c.)

M1:

$$I_{DS1} = \frac{W}{L}\frac{\mu_e C_{ox}}{\left(1+\frac{v_{DS}}{E_c L}\right)}\left(V_{GS}-V_T-\frac{V_{DS}}{2}\right)V_{DS} = (10)\frac{270(1.6\text{x}10^{-6})}{1+\frac{0.1}{0.6}}(1.2\text{-}0.4\text{-}0.05)(0.1)$$

$$I_{DS1} = (10)\frac{(270)(1.6\text{x}10^{-6})}{1.1667}(0.75)(0.1) = \underline{278\mu\text{A}} \qquad (5)$$

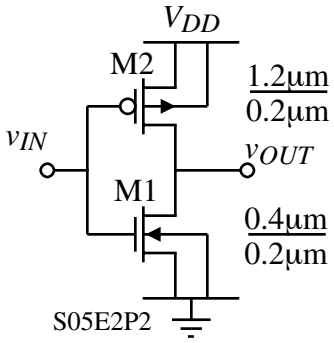
M2 (Ignore the bulk since V_{out} = 0.1V):

$$I_{DS2} = Wv_{sat}C_{ox}\frac{(V_{GS}-V_T)^2}{(V_{GS}-V_T)+E_c L}$$

$$= (0.25\text{x}10^{-4})(8\text{x}10^{6})(1.6\text{x}10^{-6})\frac{(1.7\text{-}0.1\text{-}0.4)^2}{(1.7\text{-}0.1\text{-}0.4)+0.6} = \underline{256\mu\text{A}} \qquad (5)$$

Problem 2 – (25 points)

A CMOS inverter in 0.18μm technology is shown. This inverter is to be operated from V_{DD} = 1.8V. Find the switching threshold, V_s, and sketch the voltage transfer characteristic for this case. Design the CMOS inverter (W_N /W_P) to achieve a switching threshold of $0.5V_{DD}$.



Solution

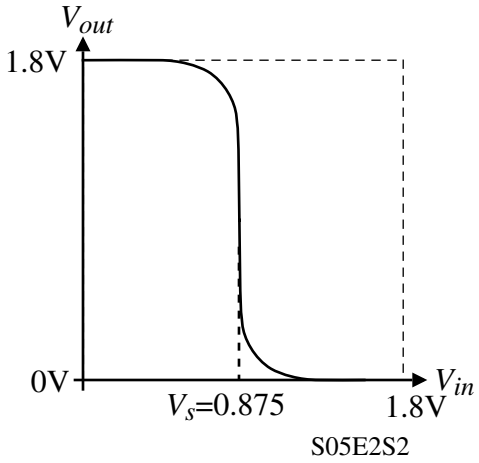
The switching threshold, V_s, is found as

$$V_s = \frac{V_{DD} - |V_{TP}| + \chi V_{TN}}{1+\chi} \text{ where } \chi = \sqrt{\frac{\mu_n W_N}{\mu_p W_P}}$$

$$\chi = \sqrt{\frac{270 \cdot 0.4}{70 \cdot 1.2}} = 1.134$$

$$\therefore \quad V_s(1.8\text{V}) = \frac{1.8\text{-}0.5+(1.134)(0.5)}{1+1.134} = \underline{\underline{0.875\text{V}}} \quad (10)$$

The VTC is shown.



To design the CMOS inverter to achieve a switching threshold of $0.5V_{DD}$, we solve for χ.to get

$$\chi = \frac{V_{DD} - |V_{TP}| - V_s}{V_s - V_{TN}} = \frac{0.5V_{DD} - |V_{TP}|}{0.5V_{DD} - V_{TN}} = 1$$

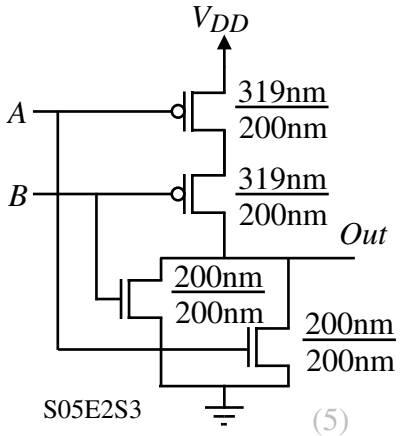
$$\therefore \sqrt{\frac{\mu_n W_N}{\mu_p W_P}} = 1 \rightarrow \frac{W_N}{W_P} = \frac{\mu_p}{\mu_n} = \underline{\underline{0.26}} \quad (10)$$

(5)

Problem 3 – (25 points)

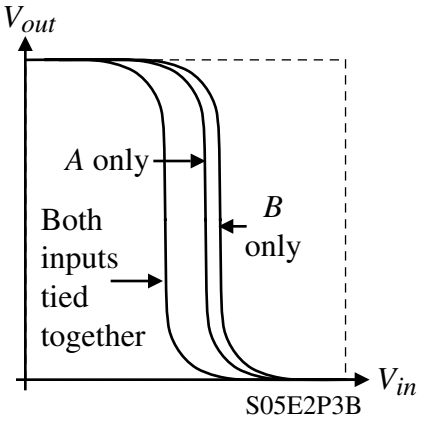
Use 0.18μm technology for this problem.

(a.) For the NOR gate shown, size the transistors to deliver a switching threshold of $V_S = 0.75$V. Place the device sizes (W) on the schematic in units of nanometers assuming $L = 200$nm. Choose the W such that $R_{pulldown}$ is the same as the standard inverter.



(5)

(b.) The voltage transfer curve of this gate is shown for various combinations of inputs. Provide an explanation as to why this occurs. How would you adjust the expression of V_s to account for this effect?



Solution

a.) $V_S = \dfrac{V_{DD} - |V_{Tp}| + \chi V_{Tn}}{1+\chi}$ where $\chi = \sqrt{\dfrac{\mu_n W_n}{\mu_p W_p}}$

$$0.75 = \frac{1.8-0.5+\chi 0.5}{1+\chi} \rightarrow 0.75+0.75\chi = 1.3 + 0.5\chi$$

$$\therefore \quad 0.25\chi = 0.55 \rightarrow \chi = 2.2$$

$$\chi^2 = \frac{\mu_n W_n}{\mu_p W_p} \rightarrow 2.2^2 = \frac{270 W_n}{70 W_p} \rightarrow \frac{W_n}{W_p} = \frac{70}{270} 2.2^2 = 1.255$$

To get the standard pull-up resistance, W_n must be 200nm. Therefore,

$W_n = 200$nm and $W_p = (1/1.255)\cdot 2 \cdot 200$nm $= 319$nm (10)

This result means that the normal $4W_n = 800$nm for the PMOS transistors is reduced to 319nm in order to achieve the lower V_s (weakening the PMOS devices).

(b.) Compared with A, B moves to the right because of the body effect on the PMOS transistor.

With both inputs tied together the pull-down is stronger because both NMOS transistors are in parallel for an effective doubling of the pull-down width. (10)

To account for the difference, adjust the value of $|V_{Tp}|$ to include the body effect.

Problem 4 – (25 points)

Using complex CMOS logic, implement the function, F = (AB+C)E. Assume that each input and its complement are available. Assuming all transistors have the same length, size the widths to implement the FO4 rules (the worst case pull-up and pull-down is identical to an inverter with $W_p = 2W$ and $W_n = W$). What is the value of W for this logic gate if $t_{PLH} = t_{PHL} = 50$ps, $L = 0.1\mu$m, and $C_L = 100$fF?

Solution

NMOS complex:

$$\overline{F} = \overline{(AB+C)E} = \overline{AB+C} + \overline{E}$$

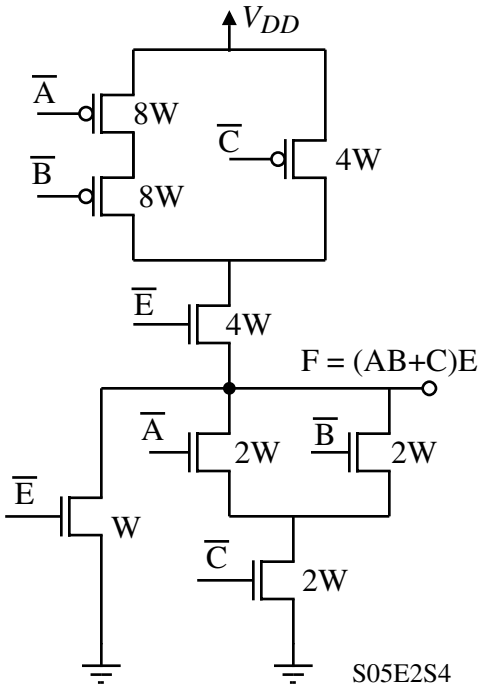
$$= \overline{AB}\,\overline{C} + \overline{E} = (\overline{A} + \overline{B})\,\overline{C} + \overline{E} \quad (8)$$

PMOS complex:

$$F = \overline{A}\,\overline{B} + \overline{C} + \overline{E} = (\overline{A}\,\overline{B} + \overline{C})\,\overline{E} \quad (8)$$

which is the dual of $\overline{F}$

Therefore, the CMOS logic implementation is shown along with the sizing that satisfies the FO4 rules.



The value of W can be found as follows,

$$t_{PHL} = t_{PLH} = 50\text{ps} = 0.7R_{eff}C_L$$

$$50\text{ps} = 0.7R_{eqn}(L/W)C_L$$

$$= 0.7(12.5\text{k}\Omega)(L/W)100\text{fF}$$

$$\therefore\ W/L = \frac{0.7\cdot 12.5\text{x}10^3\cdot 100\text{fF}}{50\text{ps}} = 17.5$$

$$W = 17.5(0.1\mu\text{m}) = \underline{\underline{1.75\mu\text{m}}} \quad (9)$$