EXAMINATION NO. 2

NAME_____SCORE_____/100

INSTRUCTIONS: This exam is closed book. You are allowed to have one page of handwritten (or typed) notes (both sides). The exam consists of 4 questions for a total of 100 points. Please show your work leading to your answers so that maximum partial credit may be given where appropriate. Be sure to turn in your exam with the problems in numerical order, firmly attached together.

TRANSISTOR INFORMATION:

The following is for an NMOS transistor only (with appropriate sign changes they can be used for PMOS transistors):

$$V_T = V_{T0} + \gamma(\sqrt{|2\phi_F| + \text{VSB}} - \sqrt{|2\phi_F|}$$

For long-channel devices, the current equations are:

If $V_{GS} \geq V_T$

and $V_{DS} \geq V_{GS} - V_T$ (the saturation region) $I_{DS} = \frac{k}{2}(V_{GS} - V_T)^2 (1+\lambda V_{DS})$

or $V_{DS} \leq V_{GS} - V_T$ (the linear region) $I_{DS} = \frac{k}{2}[2(V_{GS} - V_T)V_{DS} - V_{DS}^2]$

If $V_{GS} < V_T$ (subthreshold region) $I_{DS} \approx 0$

For velocity saturated short-channel devices, the current equations are:

If $V_{GS} \geq V_T$

and $V_{DS} \geq \frac{(V_{GS} - V_T)E_cL}{(V_{GS} - V_T) + E_cL}$ (saturation region) $I_{DS} = Wv_{sat}C_{ox}\frac{(V_{GS} - V_T)^2}{(V_{GS} - V_T) + E_cL}$

or $V_{DS} < \frac{(V_{GS} - V_T)E_cL}{(V_{GS} - V_T) + E_cL}$ (linear region) $I_{DS} = \frac{W}{L}\frac{\mu_e C_{ox}}{\left(1 + \frac{v_{DS}}{E_cL}\right)}\left(V_{GS} - V_T - \frac{V_{DS}}{2}\right)V_{DS}$

If $V_{GS} < V_T$ (subthreshold region) $I_{DS} = I_s \exp\left(\frac{q(V_{GS} - V_T - V_{offset})}{nkT}\right)\left[1 - \exp\left(\frac{-qV_{DS}}{kT}\right)\right]$

		0.18µm		0.13µm		
Name	Symbol	NMOS	PMOS	NMOS	PMOS	Units
Oxide Thickness	t_{ox}	35	35	22	22	Å
Oxide Capacitance	C_{ox}	1.0	1.0	1.6	1.6	µF/cm^2
Threshold Voltage	V_{TO}	0.5	-0.5	0.4	-0.4	V
Body-Effect Term	γ	0.3	0.3	0.2	0.2	V$^{0.5}$
Fermi Potential	$2\lvert\phi_F\rvert$	0.84	0.84	0.88	0.88	V
Junction Cap. Coeff.	C_{j0}	1.6	1.6	1.6	1.6	fF/µm^2
Built-In Junct. Potential	ϕ_B	0.9	0.9	1.0	1.0	V
Grading Coefficient	m	0.5	0.5	0.5	0.5	-
Nominal Mobility	μ_o	540	180	540	180	cm^2/V·s
Effective Mobility	μ_e	270	70	270	70	cm^2/V·s
Critical Field	E_c	6x10^4	24x10^4	6x10^4	24x10^4	V/cm
Critical Field x L	E_cL	1.2	4.8	0.6	2.4	V
Effective Resistance	R_{eff}	12.5	30	12.5	30	kΩ/sq.
Saturation Velocity	v_{sat}	8x10^6				cm/s

CAPACITOR INFORMATION:

	Cutoff	Linear	Saturation
C_{gs}	C_{ol}	$C_{ol} + 0.5C_g$	$C_{ol} + 0.67C_g$
C_{gd}	C_{ol}	$C_{ol} + 0.5C_g$	C_{ol}
C_{gb}	$1/(1/C_g+1/C_{jc})<C_{gb}< C_g$	0	0
C_{sb}	C_{jSB}	$C_{jSB} +\alpha_1 C_{jc}$	$C_{jSB} +\beta_1 C_{jc}$ (α,β small)
C_{db}	C_{jDB}	$C_{jDB} +\alpha_2 C_{jc}$	$C_{jDB} +\beta_2 C_{jc}$ (α,β small)

where, C_{ol} = overlap capacitance C_{jc} = channel to substrate depeletion capacitance

$$C_g = C_{ox} L \qquad C_j = \frac{C_{jb}(A_b+A_{sw})}{\left(1 - \frac{V_j}{\phi_B}\right)^{mj}}$$

where A_b = area of source/drain and A_{sw} = area of side of source/drain facing the channel

Gate capacitance coefficient: C_g = 2fF/μm

Self capacitance coefficient: C_{eff} = 1fF/μm

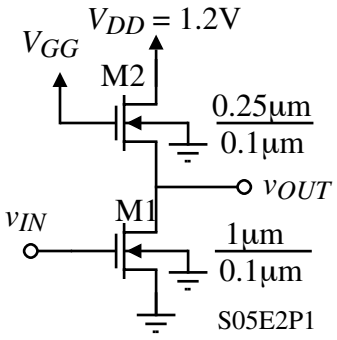
Wire capacitance coefficient: C_w = 0.1-0.25fF/μm

OTHER INFORMATION:

$\varepsilon_{ox} = 4\varepsilon_o = 4 \cdot 8.85 \text{x} 10^{-14}$ F/cm = $3.54 \text{x} 10^{-13}$ F/cm

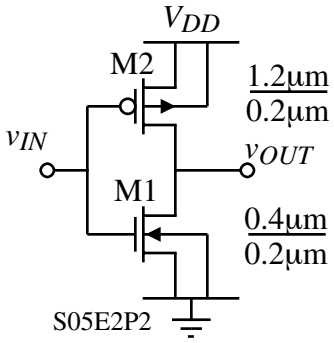
Problem 1 - (25 points)

The inverter shown is to be designed in a 0.13μm technology to have V_{OH} = 1.2V and V_{OL} = 0.1V. (a.) Find the value of V_{GG} needed to produce the desired value of V_{OH}. (b.) What is the region of operation for each transistor when the input is at V_{DD} and the output is at V_{OL} (use the value of V_{GG} found above)? (c.) How much current flows in each transistor when the input is at V_{DD} and the output is low? (The current in each transistor does not have to be equal.)



Problem 2 – (25 points)

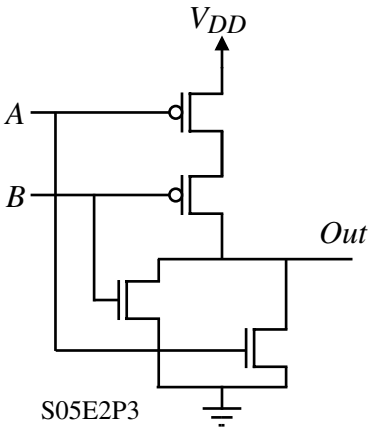
A CMOS inverter in 0.18μm technology is shown. This inverter is to be operated from V_{DD} = 1.8V. Find the switching threshold, V_s, and sketch the voltage transfer characteristic for this case. Design the CMOS inverter (W_N /W_P) to achieve a switching threshold of $0.5V_{DD}$.



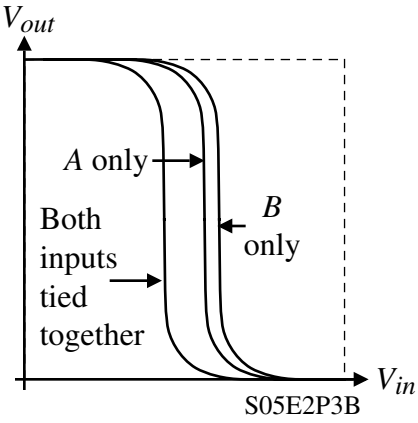
Problem 3 – (25 points)

Use 0.18μm technology for this problem.

(a.) For the NOR gate shown, size the transistors to deliver a switching threshold of $V_S = 0.75V$. Place the device sizes (W) on the schematic in units of nanometers assuming L = 200nm. Choose the W such that $R_{pulldown}$ is the same as the standard inverter.



(b.) The voltage transfer curve of this gate is shown below for various combinations of inputs. Provide an explanation as to why this occurs. How would you adjust the expression of V_s to account for this effect?



Problem 4 – (25 points)

Using complex CMOS logic, implement the function, F = (AB+C)E. Assume that each input and its complement are available. Assuming all transistors have the same length, size the widths to implement the FO4 rules (the worst case pull-up and pull-down is identical to an inverter with $W_p = 2W$ and $W_n = W$). What is the value of W for this logic gate if $t_{PLH} = t_{PHL} = 50$ps, $L = 0.1\mu$m, and $C_L = 100$fF?

Extra Sheet