EXAMINATION NO. 3

NAME_____SCORE_____/100

INSTRUCTIONS: This exam is closed book. You are allowed to have one page of handwritten (or typed) notes (both sides, no Xerox reductions). The exam consists of 4 questions for a total of 100 points. Please show your work leading to your answers so that maximum partial credit may be given where appropriate. Be sure to turn in your exam with the problems in numerical order, firmly attached together.

TRANSISTOR INFORMATION:

The following is for an NMOS transistor only (with appropriate sign changes they can be used for PMOS transistors):

$$V_T = V_{T0} + \gamma(\sqrt{|2\phi_F| + VSB} - \sqrt{|2\phi_F|}$$

For long-channel devices, the current equations are:

If $V_{GS} \geq V_T$

and $V_{DS} \geq V_{GS} - V_T$ (the saturation region) $I_{DS} = \frac{k}{2}(V_{GS} - V_T)^2 (1+\lambda V_{DS})$

or $V_{DS} \leq V_{GS} - V_T$ (the linear region) $I_{DS} = \frac{k}{2}[2(V_{GS} - V_T)V_{DS} - V_{DS}^2]$

If $V_{GS} < V_T$ (subthreshold region) $I_{DS} \approx 0$

For velocity saturated short-channel devices, the current equations are:

If $V_{GS} \geq V_T$

and $V_{DS} \geq \frac{(V_{GS} - V_T)E_c L}{(V_{GS} - V_T) + E_c L}$ (saturation region) $I_{DS} = W v_{sat} C_{ox} \frac{(V_{GS} - V_T)^2}{(V_{GS} - V_T) + E_c L}$

or $V_{DS} < \frac{(V_{GS} - V_T)E_c L}{(V_{GS} - V_T) + E_c L}$ (linear region) $I_{DS} = \frac{W}{L} \frac{\mu_e C_{ox}}{\left(1 + \frac{v_{DS}}{E_c L}\right)} \left(V_{GS} - V_T - \frac{V_{DS}}{2}\right) V_{DS}$

If $V_{GS} < V_T$ (subthreshold region) $I_{DS} = I_s \exp\left(\frac{q(V_{GS} - V_T - V_{offset})}{nkT}\right)\left[1 - \exp\left(\frac{-qV_{DS}}{kT}\right)\right]$

		0.18μm		0.13μm		
Name	Symbol	NMOS	PMOS	NMOS	PMOS	Units
Oxide Thickness	t_{ox}	35	35	22	22	Å
Oxide Capacitance	C_{ox}	1.0	1.0	1.6	1.6	μF/cm^2
Threshold Voltage	V_{TO}	0.5	-0.5	0.4	-0.4	V
Body-Effect Term	γ	0.3	0.3	0.2	0.2	V$^{0.5}$
Fermi Potential	$2\lvert\phi_F\rvert$	0.84	0.84	0.88	0.88	V
Junction Cap. Coeff.	C_{j0}	1.6	1.6	1.6	1.6	fF/μm^2
Built-In Junct. Potential	ϕ_B	0.9	0.9	1.0	1.0	V
Grading Coefficient	m	0.5	0.5	0.5	0.5	-
Nominal Mobility	μ_o	540	180	540	180	cm^2/V·s
Effective Mobility	μ_e	270	70	270	70	cm^2/V·s
Critical Field	E_c	6x10^4	24x10^4	6x10^4	24x10^4	V/cm

Critical Field x L	$E_c L$	1.2	4.8	0.6	2.4	V
Effective Resistance	R_{eff}	12.5	30	12.5	30	kΩ/sq.
Saturation Velocity	v_{sat}	$8\text{x}10^6$				cm/s

CAPACITOR INFORMATION:

	Cutoff	Linear	Saturation
C_{gs}	C_{ol}	$C_{ol} + 0.5C_g$	$C_{ol} + 0.67C_g$
C_{gd}	C_{ol}	$C_{ol} + 0.5C_g$	C_{ol}
C_{gb}	$1/(1/C_g+1/C_{jc}) < C_{gb} < C_g$	0	0
C_{sb}	C_{jSB}	$C_{jSB} + \alpha_1 C_{jc}$	$C_{jSB} + \beta_1 C_{jc}$ (α,β small)
C_{db}	C_{jDB}	$C_{jDB} + \alpha_2 C_{jc}$	$C_{jDB} + \beta_2 C_{jc}$ (α,β small)

where, C_{ol} = overlap capacitance C_{jc} = channel to substrate depeletion capacitance

$$C_g = C_{ox} L \qquad C_j = \frac{C_{jb}(A_b + A_{sw})}{\left(1 - \frac{V_j}{\phi_B}\right)^{mj}}$$

where A_b = area of source/drain and A_{sw} = area of side of source/drain facing the channel

Gate capacitance coefficient: $C_g = C_{ox}L + 2C_{ol} \approx 2fF/\mu m$

Self capacitance coefficient: $C_{eff} = C_j + 2C_{ol} \approx 1fF/\mu m$

Wire capacitance coefficient: $C_w = C_{int} =$ 0.1-0.25fF/μm

OTHER INFORMATION:

$\varepsilon_{ox} = 4\varepsilon_o = 4 \cdot 8.85\text{x}10^{-14}$ F/cm = $3.54\text{x}10^{-13}$ F/cm

Logical Effort:

Type of Gate	1 input	2 inputs	3 inputs	4 inputs
Inverter	1	-	-	-
NAND	-	4/3	5/3	6/3
NOR	-	5/3	7/3	9/3

Parasitic Terms:

Type of Gate	1 input	2 inputs	3 inputs	4 inputs
Inverter	1/2	-	-	-
NAND	-	1	3/2	2
NOR	-	3/2	9/4	3