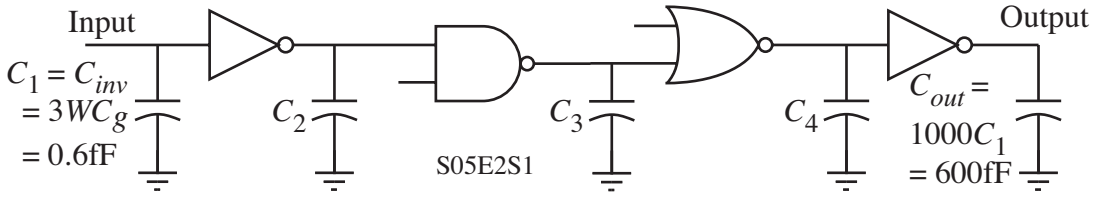
EXAMINATION NO. 3 - SOLUTIONS

(Average Score = 77/100)

Problem 1 - (25 points)

Calculate the optimum delay (in ps) and the size of the transistors (W and L in μm) for the logic circuit shown. All devices are standard CMOS and all transistors have a minimum length of $L = 0.1\mu$m. C_{inv} is the input capacitance of a minimum size inverter.



Solution

Use logical effort to find the capacitances and the delay.

$$PE = \Pi(LE \cdot FO) = (1)\left(\frac{4}{3}\right)\left(\frac{5}{3}\right)(1)\,(1000) = 2222$$

$$SE = (PE)^{1/N} = (2222)^{1/4} = 6.87$$

$$C_4 = \frac{LE \cdot C_{out}}{SE} = \frac{(1)(600\text{fF})}{6.87} = 87.34\text{fF}$$

$$87.34 = 3WC_g \quad \rightarrow \quad W_n = W = \frac{87.34}{3 \cdot 2} = \underline{14.56\mu\text{m}} \qquad W_p = 2\,W_n = \underline{29.11\mu\text{m}}$$

$$C_3 = \frac{LE \cdot C_4}{SE} = \frac{(\frac{5}{3})(87.34\text{fF})}{6.87} = 21.19\text{fF}$$

$$21.19 = 5WC_g \quad \rightarrow \quad W_n = W = \frac{21.19}{5 \cdot 2} = \underline{2.12\mu\text{m}} \qquad W_p = 4\,W_n = \underline{8.48\mu\text{m}}$$

$$C_2 = \frac{LE \cdot C_3}{SE} = \frac{(\frac{4}{3})(21.19\text{fF})}{6.87} = 4.11\text{fF}$$

$$4.11 = 4WC_g \quad \rightarrow \quad W = \frac{4.11}{4 \cdot 2} = 0.514\mu\text{m} \qquad W_n = W_p = 2W = \underline{1.03\mu\text{m}}$$

$$C_1 = \frac{LE \cdot C_2}{SE} = \frac{(1)(4.11\text{fF})}{6.87} = 0.6\text{fF}$$

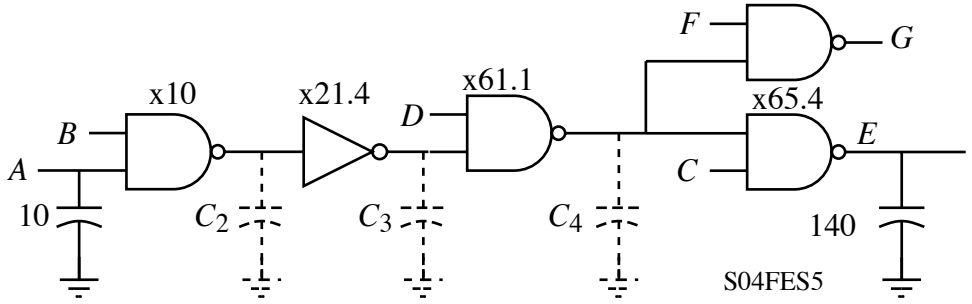
$$0.6 = 3WC_g \quad \rightarrow \quad W_n = W = \frac{0.6}{3 \cdot 2} = \underline{0.1\mu\text{m}} \qquad W_p = 2W_n = \underline{0.2\mu\text{m}}$$

$$D = \sum_1^N (SE + P_N) = \sum_1^4 (SE + P_N) = 4(6.87) + 0.5 + 1 + 1.5 + 0.5 = 31$$

$$\tau = 3R_{eqn}C_gL_n = 3(12.5\text{K})(2\text{fF})(0.1\mu\text{m}) = 7.5\text{ps} \qquad \therefore \qquad \text{Delay} = 31 \cdot 7.5\text{ps} = \underline{232.5\text{ps}}$$

Problem 2 – (25 points)

What is the minimum possible delay through the following circuit from node *A* to node *E*, and how would you size the gates? You can leave the delay and sizes in unitless quantities. Assume that the two NAND gates at the output are the same size.



Solution

$LE = (4/3) \times (1) \times (4/3) \times (4/3) = (4/3)^3$

$BE = (1) \times (1) \times (1) \times (2) = 2$

$FO = \frac{140}{10} = 14$

$\therefore \quad PE = (4/3)^3(2)(14) = 66.4 \quad \rightarrow \quad SE = (PE)^{1/4} = 2.854$

$C_4 = \frac{140(4/3)}{2.854} = \underline{65.4} \qquad 4WC_g = 65.4 \rightarrow \quad W = 8.19 \rightarrow W_n = W_p = 8.19$

$C_3 = \frac{2 \cdot 65.4(4/3)}{2.854} = \underline{61.1} \qquad 4WC_g = 61.1 \rightarrow \quad W = 7.66 \rightarrow W_n = W_p = 7.66$

$C_2 = \frac{61.1(1)}{2.854} = \underline{21.4} \qquad 3WC_g = 21.4 \rightarrow \quad W = 3.56 \rightarrow W_n = 3.56 \;\; W_p = 7.17$

$C_{in} = \frac{21.4(4/3)}{2.854} = 10 \qquad 4WC_g = 10 \rightarrow \quad W = 1.25 \rightarrow W_n = W_p = 1.25$

$D = 4(2.854) + 3(1) + (0.5) = \underline{14.91}$

Problem 3 – (25 points)

Using transmission gates, design a logic circuit whose output is,

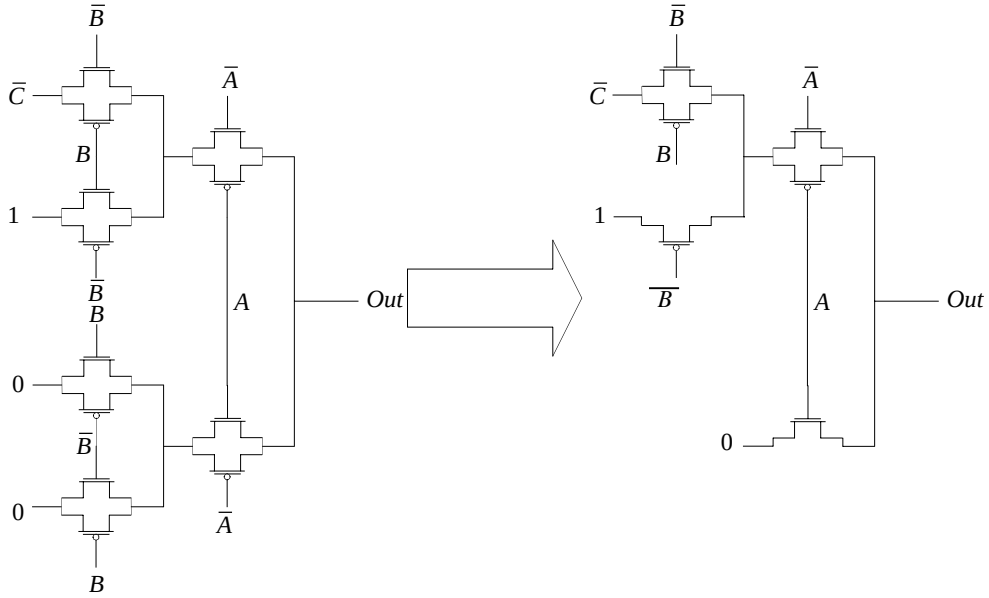
$$Out = \overline{(A + B + C)} + \overline{A}\,B$$

Use *A* and *B* as the control signals of a two-level multiplexer architecture. Remove the transistors and switches that are not necessary.

Solution

$$Out = \overline{(A + B + C)} + \overline{A}B = \overline{A}\,\overline{B}\,\overline{C} + \overline{A}B$$

A	B	C	Out
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0



Problem 4 – (25 points)

Design a domino logic circuit whose output is

$$Out = A\overline{B} + BC + \overline{C}$$

Solution