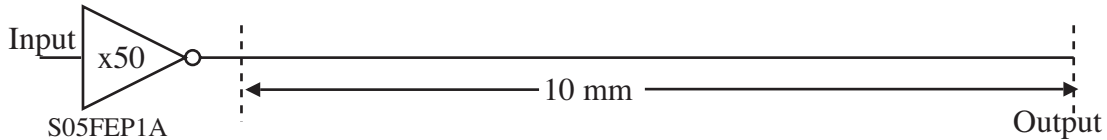


FINAL EXAMINATION
(Average score = 82/100)

Problem 1 - (20 points – This problem is required)

a.) An interconnect line is 10 mm long, 0.5μm wide, and has a resistance of 27mΩ/sq. and a capacitance of 0.1fF/μm and is driven by a 50X inverter (an inverter with an 200λ PMOS and a 100λ NMOS where λ = 0.1μm and L = 2λ). What is the total delay of the circuit as calculated from the Elmore delay assuming the pi model for the wire from the input of the inverter to the end of the interconnect line?



b.) Divide the 10mm wire above into 5 equal segments and use a buffer of x50 to drive each segment (use the existing buffer to drive the first segment). Find the new propagation delay calculated from the Elmore delay.

Solution

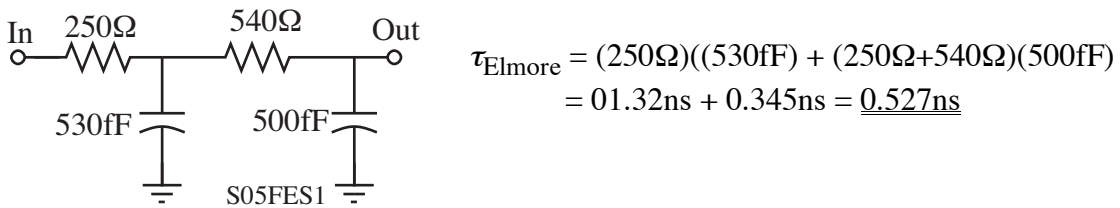
$$a.) R_{wire} = R_{int}L = \left(\frac{0.027\Omega/sq.}{0.5\mu m}\right)(10,000\mu m) = 540\Omega$$

$$C_{wire} = C_{int}L = (0.1fF/\mu m)(10,000\mu m) = 1pF$$

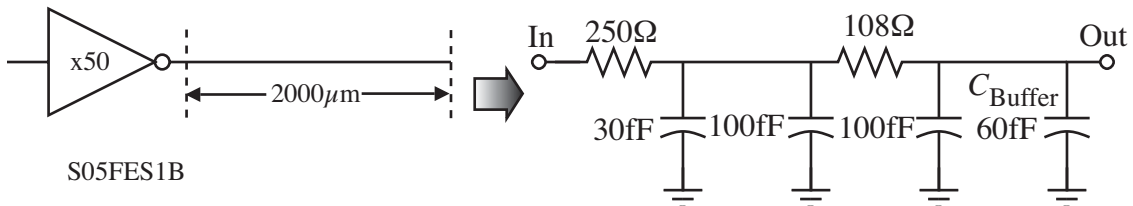
$$\text{The inverter on resistance is } R_{eff} = \frac{R_{eqn}}{50} = \frac{12.5k\Omega}{50} = 250\Omega$$

$$\text{The inverter output capacitance is, } C_{self} = C_{eff}(2W+W)50 = (1fF/\mu m)(0.6\mu m)50 = 30fF$$

The model for this part is given as,



b.) The model for one segment is given as,



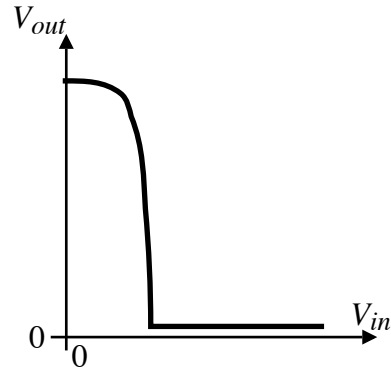
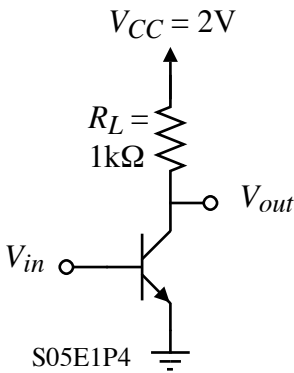
$$C_{Buffer} = C_g(2W+W)50 = 2fF/\mu m(0.6\mu m)50 = 60fF$$

$$\tau_{Elmore} = 5[(250\Omega)((130fF) + (250\Omega + 108\Omega)(160fF))] = 5(0.08978ns) = \underline{0.449ns}$$

Problem 2 – (20 points – This problem is optional)

A bipolar-resistor inverter is shown along with the generic voltage transfer function. Use the large signal model of the BJT and the circuit to find values for V_{OH} , V_{OL} , V_{IL} , and V_{IH} . The large signal model for the BJT is

$$I_c = I_s \exp\left(\frac{V_{in}}{V_t}\right)$$



where $I_s = 1\text{fA}$ and $V_t = 25\text{mV}$. The collector-emitter saturation voltage of the BJT is $V_{CE}(\text{sat}) = 0.2\text{V}$. Use this information to find the values of NM_H and NM_L .

Solution

Note that $V_{OH} = V_{CC} = \underline{2\text{V}}$ and $V_{OL} = V_{CE}(\text{sat}) = \underline{0.2\text{V}}$.

The output voltage can be expressed as,

$$V_{out} = V_{CC} - I_c R_L = 2 - R_L I_s \exp\left(\frac{V_{in}}{V_t}\right)$$

To find V_{IL} , set $dV_{out}/dV_{in} = -1$.

$$\frac{dV_{out}}{dV_{in}} = -\frac{R_L I_s}{V_t} \exp\left(\frac{V_{in}}{V_t}\right) \quad \rightarrow \quad -1 = -\frac{R_L I_s}{V_t} \exp\left(\frac{V_{IL}}{V_t}\right)$$

Thus, $V_{IL} = V_t \ln\left(\frac{V_t}{R_L I_s}\right) = 25\text{mV} \ln\left(\frac{25\text{mV}}{1\text{k}\Omega \cdot 1\text{fA}}\right) = 25\text{mV}(17.03) = \underline{0.426\text{V}}$

Let $V_{out} = 0.2\text{V}$ to find V_{IH} .

$$0.2\text{V} = 2 - R_L I_s \exp\left(\frac{V_{IH}}{V_t}\right) \quad \rightarrow \quad V_{IH} = V_t \ln(1.8 \times 10^9) = 25\text{mV}(21.31) = \underline{0.533\text{V}}$$

Therefore,

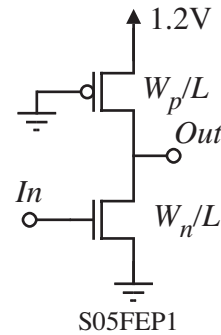
$$NM_H = V_{OH} - V_{IH} = 2\text{V} - 0.533\text{V} = \underline{1.467\text{V}}$$

and

$$NM_L = V_{IL} - V_{OL} = 0.426\text{V} - 0.2\text{V} = \underline{0.226\text{V}}$$

Problem 3 – (20 points – This problem is optional)

Design a pseudo-NMOS inverter in $0.13\mu\text{m}$ technology to give $V_{OH} = V_{DD} = 1.2\text{V}$ and $V_{OL} = 0.1\text{V}$. Assume $L = 200\text{nm}$ and find the value of the W 's if $W_p = 200\text{nm}$. Assume $v_{sat} = 8 \times 10^6 \text{ cm/s}$.

Solution

Assume the PMOS is saturated and the NMOS is linear.

Thus,

$$\frac{W_p v_{sat} C_{ox} (V_{DD} - |V_{Tp}|)^2}{V_{DD} - V_{Tp} + E_{cp} L_p} = \frac{W_n}{L_n} \frac{\mu_n C_{ox}}{\left(1 + \frac{V_{OL}}{E_{cn} L_n}\right) \left[(V_{DD} - V_{Tn}) V_{OL} - \frac{V_{OL}^2}{2}\right]}$$

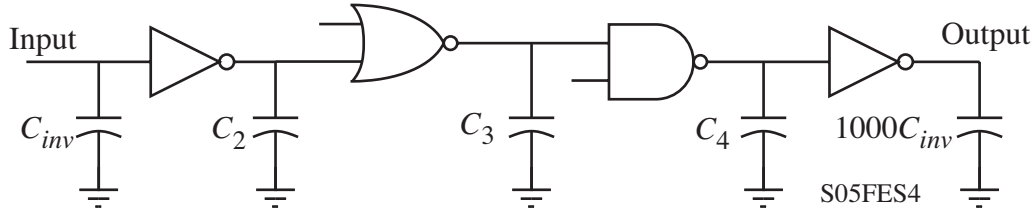
Substituting values,

$$W_p \frac{(8 \times 10^6 \text{ cm/s})(1.6 \mu\text{F/cm}^2)(1.2 - 0.4)^2}{1.2 - 0.4 + 2.4} = \frac{W_n}{0.2 \times 10^{-4}} \frac{(270)(1.6 \times 10^{-6})}{\left(1 + \frac{0.1}{0.6}\right)} \left[(1.2 - 0.4)(0.1) - \frac{0.01}{2}\right]$$

$$2.56 W_p = 1.3886 W_n \rightarrow \frac{W_n}{W_p} = 1.853 \rightarrow W_n = 1,843.299 \text{ nm} = \underline{\underline{369 \text{ nm}}}$$

Problem 4 - (25 points)

Calculate the optimum delay (in ps) and the size of the transistors (in μm) for the logic circuit shown. All devices are standard CMOS and all transistors have a minimum length of $L = 0.1\mu\text{m}$. C_{inv} is the input capacitance of a minimum size inverter ($W = 0.2\mu\text{m}$).

Solution

$$C_{inv} = 3WC_g = 3(0.2\mu\text{m})(2\text{fF}/\mu\text{m}) = 1.2\text{fF}$$

Use logical effort to find the capacitances and the delay.

$$PE = \Pi(LE \cdot FO) = (1)\left(\frac{4}{3}\right)\left(\frac{5}{3}\right)(1)(1000) = 2222$$

$$SE = (PE)^{1/N} = (2222)^{1/4} = 6.87$$

$$C_4 = \frac{LE \cdot C_{out}}{SE} = \frac{(1)(1200\text{fF})}{6.87} = 175\text{fF}$$

$$175 = 3WC_g \quad \rightarrow \quad W_n = W = \frac{175}{3 \cdot 2} = \underline{29.11\mu\text{m}} \quad W_p = 2W_n = \underline{58.22\mu\text{m}}$$

$$C_3 = \frac{LE \cdot C_4}{SE} = \frac{\frac{4}{3}(175\text{fF})}{6.87} = 33.9\text{fF}$$

$$33.9 = 4WC_g \quad \rightarrow \quad W = \frac{33.9}{4 \cdot 2} = \underline{4.24\mu\text{m}} \quad W_p = W_n = 2W = \underline{8.48\mu\text{m}}$$

$$C_2 = \frac{LE \cdot C_3}{SE} = \frac{\frac{5}{3}(33.9\text{fF})}{6.87} = 8.22\text{fF}$$

$$8.22 = 5WC_g \quad \rightarrow \quad W_n = W = \frac{8.22}{5 \cdot 2} = 0.822\mu\text{m} \quad W_p = 4W = \underline{3.29\mu\text{m}}$$

$$C_1 = \frac{LE \cdot C_2}{SE} = \frac{(1)(8.22\text{fF})}{6.87} = 1.2\text{fF}$$

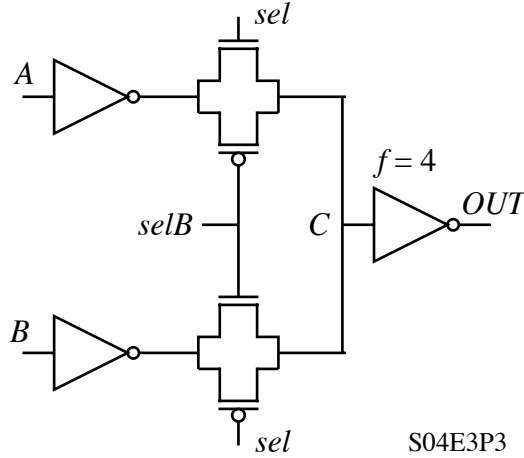
$$1.2 = 3WC_g \quad \rightarrow \quad W_n = W = \frac{1.2}{3 \cdot 2} = \underline{0.2\mu\text{m}} \quad W_p = 2W_n = \underline{0.4\mu\text{m}}$$

$$D = \sum_{1}^N (SE + P_N) = \sum_{1}^4 (SE + P_N) = 4(6.87) + 0.5 + 1 + 1.5 + 0.5 = 31$$

$$\tau = 3R_{eqn}C_gL_n = 3(12.5\text{K})(2\text{fF})(0.1\mu\text{m}) = 7.5\text{ps} \quad \therefore \quad \text{Delay} = 31 \cdot 7.5\text{ps} = \underline{232.5\text{ps}}$$

Problem 5 – (20 points – This problem is optional)

For the logic circuit shown below, assume that the transmission gates are all $4\lambda:2\lambda$ and that the inverters driving the transmission gates have PMOS transistors that are $8\lambda:2\lambda$, and NMOS transistors that are $4\lambda:2\lambda$, where $\lambda = 0.1\mu\text{m}$. The output inverter is to drive a 50 fF load. The output inverter is 4 times larger than the input inverters.



(a.) Write the logic expression for the output function in terms of A , B , sel , and $selB$.

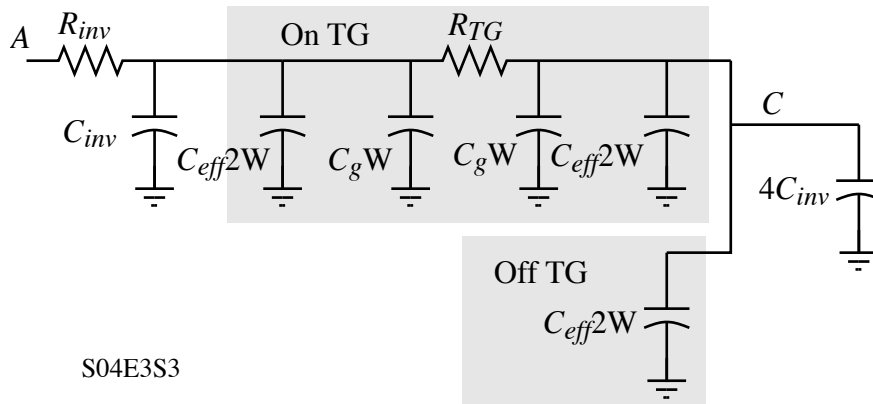
(b.) Draw an equivalent RC circuit model for the path from A to C assuming that the sel signal is high. Write down the individual contributions for each resistance and capacitance and place the total values at the appropriate nodes.

(c.) Find the Elmore delay from A to C .

Solution

(a.) $OUT = \overline{sel \cdot A} + \overline{sel \cdot B} = (\overline{sel} + A) \cdot (sel + B) = A \cdot sel + B \cdot selB$

(b.) The equivalent RC circuit model is shown below.



The quantities in this model are:

$$R_{inv} = 12.5\text{k}\Omega \left(\frac{2\lambda}{4\lambda}\right) = 6.25\text{k}\Omega, C_{inv} = C_{eff}(W_n + W_p) = 1\text{fF}/\mu\text{m}(0.4\mu\text{m} + 0.8\mu\text{m}) = 1.2\text{fF},$$

$$C_{eff}(2W) = 1\text{fF}/\mu\text{m}(0.8\mu\text{m}) = 0.8\text{fF}, C_g W = 2\text{fF}/\mu\text{m}(0.4\mu\text{m}) = 0.8\text{fF}$$

$$R_{TG} = 12.5\text{k}\Omega \left(\frac{2\lambda}{4\lambda}\right) = 6.25\text{k}\Omega, \text{ and } 4C_{inv} = 4C_g W = 4(2\text{fF}/\mu\text{m})(1.2\mu\text{m}) = 9.6\text{fF}$$

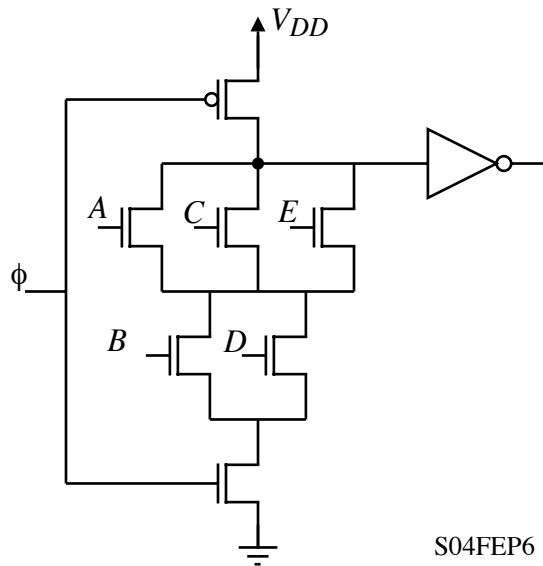
(c.) The Elmore delay from A to C is given as

$$t_{AC} = 6.25\text{k}\Omega(1.2\text{fF} + 0.8\text{fF} + 0.8\text{fF}) + (6.25\text{k}\Omega + 6.25\text{k}\Omega)(0.8\text{fF} + 0.8\text{fF} + 0.8\text{fF} + 9.6\text{fF})$$

$$= 6.25\text{k}\Omega(2.8\text{fF}) + 6.25\text{k}\Omega(12\text{fF}) = 17.5\text{ps} + 150\text{ps} = \underline{167.5\text{ps}}$$

Problem 6 – (20 points – This problem is optional)

A dynamic logic gate is shown. The pre-charge device has a W/L of 5, the n-channel devices have a W/L of 3, and inverter has a pull-up of 4 and a pull-down of 1. (a.) What is the logic function of the gate at the output of the inverter? (b.) Why is the output inverter skewed? (c.) Using the device sizes above, what is the logical effort of input B of the first stage of the domino logic (when its immediate output is falling), and the inverter (when its output is rising). Compute these two values separately.



S04FEP6

Solution

(a.) $f = (B+D)(A+C+E)$

(b.) To make the risetime faster.

(c.) B input:

The W/L of each transistor is 3 times the minimum size so the resistance of each of these transistors is $R/3$. However, there are three of them in series in the pulldown path so the effective output resistance is $3R/3 = R$. The input capacitance is 5 times the minimum capacitance. Therefore,

$$LE_B = \frac{(R)(3C_g)}{3RC_g} = 1 \quad \rightarrow \underline{\underline{LE_B = 1}}$$

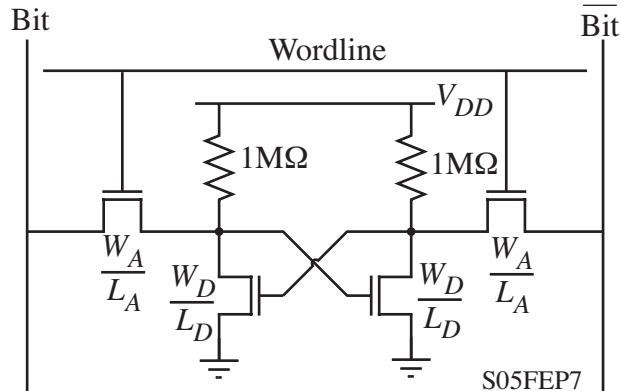
Inverter input:

For the standard inverter, the input capacitance is $3C_g$ and the output resistance is R . However, the pullup is twice as big as usual so its output resistance is $R/2$ instead of R . Therefore,

$$LE_{inv} = \frac{(R/2)(5C_g)}{3RC_g} = 5/6 \quad \rightarrow \underline{\underline{LE_{inv} = 5/6}}$$

Problem 7 – (20 points – This problem is optional)

Design the values of the access and pull-down transistor in the memory cell shown. Assume you are designing a 256x256 memory array and that the bit lines must change by 150mV in 300ps at which point the sense amplifier is activated. The total capacitance of the bit lines are 450fF each. Assume that $W_D/W_A = 1.5$. Be sure to state any other assumptions you use in working this problem. $V_{DD} = 1.2V$.

Solution

Both gates are tied to V_{DD} as shown.

The current required by this combination is,

$$I = C(\Delta V/\Delta t) = 450\text{fF}(150\text{mV}/300\text{ps}) = 225\mu\text{A}$$

Letting this current be the current through the access transistor and assuming the voltage at q , $V_q = 0.1V$ gives W_A as,

$$225\mu\text{A} \approx \frac{W_A(8 \times 10^6)(1.6\mu\text{F})(1.2-0.1-0.4)^2}{(1.2-0.1-0.4) + 0.6} = 4.825 W_A$$

$$W_A = \frac{225\mu\text{A}}{4.825} = 0.000047 \text{ cm} = \underline{0.47\mu\text{m}} \quad \text{and} \quad W_D = 1.5 W_A = \underline{0.705\mu\text{m}}$$

