FINAL EXAMINATION

NAME_____SCORE_____/100

Problem	⓵	2	3	4	5	6	7	Sum
Points								

INSTRUCTIONS: This exam is closed book. You are permitted four sheets of notes (three of which are your sheets for the 3 midterms plus a new sheet for the final exam). There should be no xerox reductions on your note sheets. The exam consists of 7, 20-point problems of which you are to work only 5 for a total of 100 points. Problem 1 must be worked and you may choose any four of the last six problems for a total of five problems. Please circle the number in the table above of the five problems you wish graded. If you do not indicate the problems to be graded, then problems 1 through 5 will be graded regardless of whether they are worked or not. Be sure to turn in only the 5 problems you wish graded in proper numerical order. Please show your work leading to your answers so that maximum partial credit may be given where appropriate.

TRANSISTOR INFORMATION:

The following is for an NMOS transistor only (with appropriate sign changes they can be used for PMOS transistors):

$$V_T = V_{T0} + \gamma(\sqrt{|2\phi_F| + VSB} - \sqrt{|2\phi_F|}$$

For long-channel devices, the current equations are:

If $V_{GS} \geq V_T$

and $V_{DS} \geq V_{GS} - V_T$ (the saturation region) $\quad I_{DS} = \frac{k}{2}(V_{GS} - V_T)^2 (1+\lambda V_{DS})$

or $V_{DS} \leq V_{GS} - V_T$ (the linear region) $\quad I_{DS} = \frac{k}{2}[2(V_{GS} - V_T)V_{DS} - V_{DS}^2]$

If $V_{GS} < V_T$ (subthreshold region) $\quad I_{DS} \approx 0$

For velocity saturated short-channel devices, the current equations are:

If $V_{GS} \geq V_T$

and $V_{DS} \geq \frac{(V_{GS} - V_T)E_cL}{(V_{GS} - V_T) + E_cL}$ (saturation region) $I_{DS} = Wv_{sat}C_{ox}\frac{(V_{GS} - V_T)^2}{(V_{GS} - V_T) + E_cL}$

or $V_{DS} < \frac{(V_{GS} - V_T)E_cL}{(V_{GS} - V_T) + E_cL}$ (linear region) $I_{DS} = \frac{W}{L}\frac{\mu_e C_{ox}}{\left(1+\frac{v_{DS}}{E_cL}\right)}\left(V_{GS} - V_T - \frac{V_{DS}}{2}\right)V_{DS}$

If $V_{GS} < V_T$ (subthreshold region) $\quad I_{DS} = I_s \exp\left(\frac{q(V_{GS} - V_T - V_{offset})}{nkT}\right)\left[1 - \exp\left(\frac{-qV_{DS}}{kT}\right)\right]$

		0.18μm		0.13μm		
Name	Symbol	NMOS	PMOS	NMOS	PMOS	Units
Oxide Thickness	t_{ox}	35	35	22	22	Å
Oxide Capacitance	C_{ox}	1.0	1.0	1.6	1.6	μF/cm^2
Threshold Voltage	V_{TO}	0.5	-0.5	0.4	-0.4	V
Body-Effect Term	γ	0.3	0.3	0.2	0.2	V$^{0.5}$
Fermi Potential	$2\|\phi_F\|$	0.84	0.84	0.88	0.88	V

Junction Cap. Coeff.	C_{j0}	1.6	1.6	1.6	1.6	fF/μm^2
Built-In Junct. Potential	ϕ_B	0.9	0.9	1.0	1.0	V
Grading Coefficient	m	0.5	0.5	0.5	0.5	-
Nominal Mobility	μ_o	540	180	540	180	cm^2/V·s
Effective Mobility	μ_e	270	70	270	70	cm^2/V·s
Critical Field	E_c	6x10^4	24x10^4	6x10^4	24x10^4	V/cm
Critical Field x L	E_cL	1.2	4.8	0.6	2.4	V
Effective Resistance	R_{eff}	12.5	30	12.5	30	kΩ/sq.
Saturation Velocity	v_{sat}	8x10^6				cm/s

CAPACITOR INFORMATION:

	Cutoff	Linear	Saturation
C_{gs}	C_{ol}	$C_{ol} + 0.5C_g$	$C_{ol} + 0.67C_g$
C_{gd}	C_{ol}	$C_{ol} + 0.5C_g$	C_{ol}
C_{gb}	$1/(1/C_g+1/C_{jc})<C_{gb}< C_g$	0	0
C_{sb}	C_{jSB}	$C_{jSB} +\alpha_1 C_{jc}$	$C_{jSB} +\beta_1 C_{jc}$ (α,β small)
C_{db}	C_{jDB}	$C_{jDB} +\alpha_2 C_{jc}$	$C_{jDB} +\beta_2 C_{jc}$ (α,β small)

where, C_{ol} = overlap capacitance C_{jc} = channel to substrate depeletion capacitance

$$C_g = C_{ox} L \qquad C_j = \frac{C_{jb}(A_b+A_{sw})}{\left(1- \frac{V_j}{\phi_B}\right)^{mj}}$$

where A_b = area of source/drain and A_{sw} = area of side of source/drain facing the channel

Gate capacitance coefficient: $C_g = C_{ox}L + 2C_{ol} \approx 2fF/\mu$m

Self capacitance coefficient: $C_{eff} = C_j + 2C_{ol} \approx 1$fF/$\mu$m

Wire capacitance coefficient: $C_w = C_{int} = 0.1$fF/μm

OTHER INFORMATION:

$\varepsilon_{ox} = 4\varepsilon_o = 4 \cdot 8.85\text{x}10^{-14}$ F/cm = 3.54x10^{-13} F/cm

Logical Effort:

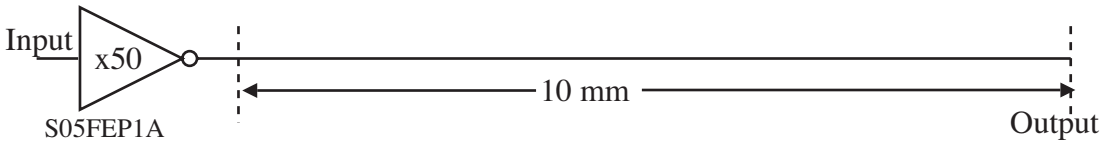
Type of Gate	1 input	2 inputs	3 inputs	4 inputs
Inverter	1	-	-	-
NAND	-	4/3	5/3	6/3
NOR	-	5/3	7/3	9/3

Parasitic Terms:

Type of Gate	1 input	2 inputs	3 inputs	4 inputs
Inverter	1/2	-	-	-
NAND	-	1	3/2	2
NOR	-	3/2	9/4	3

Problem 1 - (20 points – This problem is required)

a.) a.) An interconnect line is 10 mm long, 0.5μm wide, and has a resistance of 27mΩ/sq. and a capacitance of 0.1fF/μm and is driven by a 50X inverter (an inverter with an 200λ PMOS and a 100λ NMOS where λ = 0.1μm and L = 2λ). What is the total delay of the circuit as calculated from the Elmore delay assuming the pi model for the wire from the input of the inverter to the end of the interconnect line?

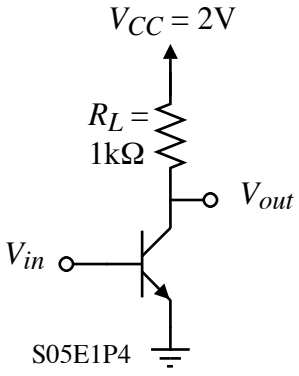


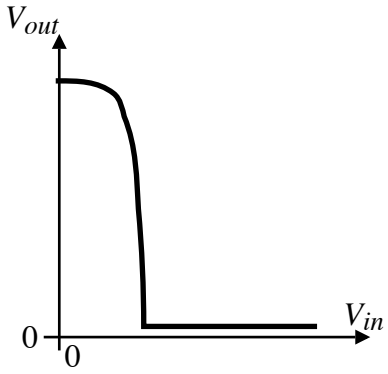
b.) Divide the 10mm wire above into 5 equal segments and use a buffer of x50 to drive each segment (use the existing buffer to drive the first segment). Find the new propagation delay calculated from the Elmore delay.

Problem 2 – (20 points – This problem is optional)

A bipolar-resistor inverter is shown along with the generic voltage transfer function. Use the large signal model of the BJT and the circuit to find values for V_{OH}, V_{OL}, V_{IL}, and V_{IH}. The large signal model for the BJT is

$$I_c = I_s \exp\left(\frac{V_{in}}{V_t}\right)$$

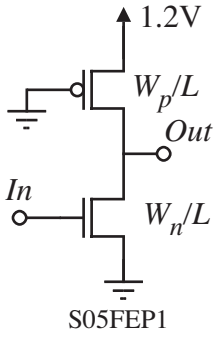




where I_s = 1fA and V_t = 25mV. The collector-emitter saturation voltage of the BJT is V_{CE}(sat) = 0.2V. Use this information to find the values of NM_H and NM_L.

Problem 3 – (20 points – This problem is optional)

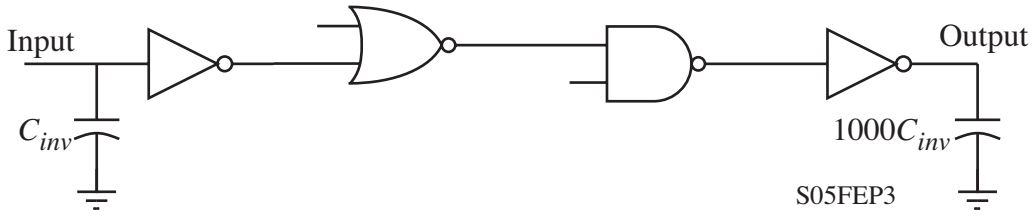
Design a pseudo-NMOS inverter in 0.13μm technology to give V_{OH} = V_{DD} = 1.2V and V_{OL} = 0.1V. Assume L = 200nm and find the value of the W's if W_p = 200nm. Assume v_{sat} = 8x10^6 cm/s.



S05FEP1

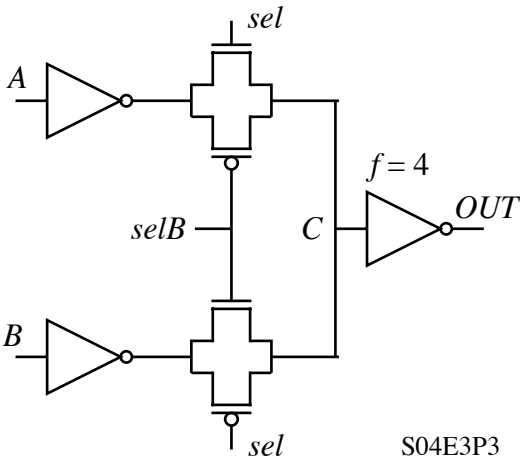
Problem 4 - (25 points)

Calculate the optimum delay (in ps) and the size of the transistors (in μm) for the logic circuit shown. All devices are standard CMOS and all transistors have a minimum length of $L = 0.1\mu$m. C_{inv} is the input capacitance of a minimum size inverter ($W = 0.2\mu$m).



Problem 5 – (20 points – This problem is optional)

For the logic circuit shown below, assume that the transmission gates are all 4λ:2λ and that the inverters driving the transmission gates have PMOS transistors that are 8λ:2λ, and NMOS transistors that are 4λ:2λ, where $\lambda = 0.1\mu$m. The output inverter is to drive a 50 fF load. The output inverter is 4 times larger than the input inverters.



S04E3P3

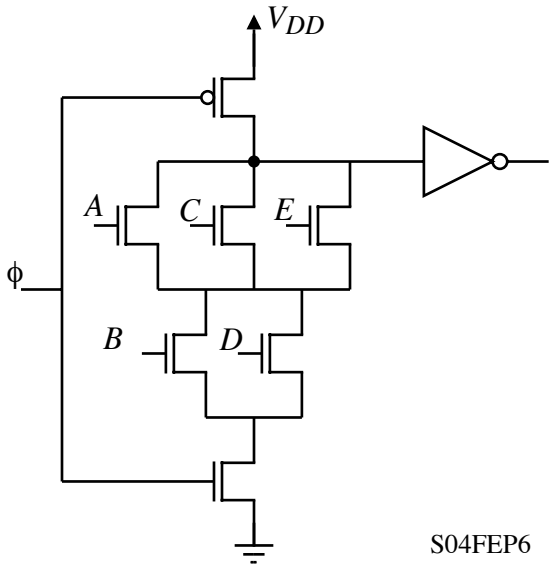
(a.) Write the logic expression for the output function in terms of *A*, *B*, *sel*, and *selB*.

(b.) Draw an equivalent *RC* circuit model for the path from *A* to *C* assuming that the *sel* signal is high. Write down the individual contributions for each resistance and capacitance and place the total values at the appropriate nodes.

(c.) Find the Elmore delay from *A* to *C*.

Problem 6 – (20 points – This problem is optional)

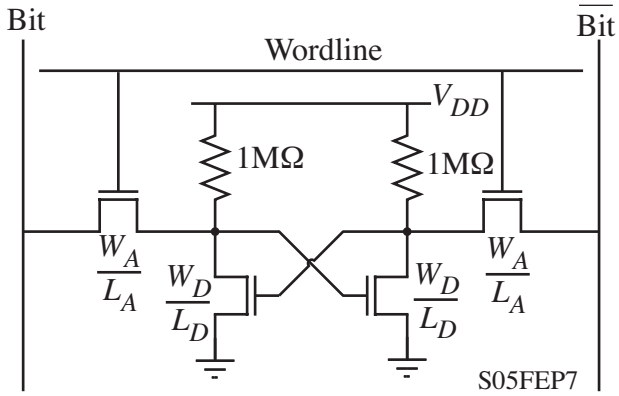
A dynamic logic gate is shown. The pre-charge device has a W/L of 5, the n-channel devices have a W/L of 3, and inverter has a pull-up of 4 and a pull-down of 1. (a.) What is the logic function of the gate at the output of the inverter? (b.) Why is the output inverter skewed? (c.) Using the device sizes above, what is the logical effort of input *B* of the first stage of the domino logic (when its immediate output is falling), and the inverter (when its output is rising). Compute these two values separately.



S04FEP6

Problem 7 – (20 points – This problem is optional)

Design the values of the access and pull-down transistor in the memory cell shown. Assume you are designing a 256x256 memory array and that the bit lines must change by 150mV in 300ps at which point the sense amplifier is activated. The total capacitance of the bit lies are 450fF each. Assume that W_D/W_A = 1.5. Be sure to state any other assumptions you use in working this problem. W_A. V_{DD} = 1.2V.



Extra Sheet