Homework No. 6 – Solutions

Problem 1 – P5.9

For t_{PLH}, we need to size the pull-up PMOS appropriately.

$$t_{PLH} = 0.7RC = 0.7R_{eqp}\frac{L}{W}C_{LOAD}$$

$$W_p = 0.7R_{SQ}\frac{L}{t_{PLH}}C_{LOAD} = 0.7(30k\Omega)\frac{(2\lambda)}{(50\times10^{-12})}(100\times10^{-15}) = 84\lambda$$

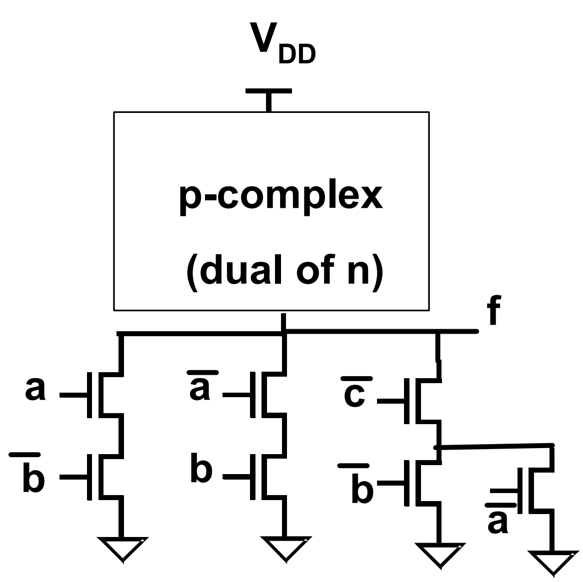
For V_{OL}:

$$I_P(sat) = \frac{W_P v_{sat} C_{OX}(V_{GS}-V_T)^2}{V_{GS}-V_T+E_{CP}L} = \frac{(4.2\times10^{-4})(8\times10^{6})(1.6\times10^{-6})(1.2-0.4)^2}{1.2-0.4+(24)(0.1)} = 1.08\text{mA}$$

$$I_P(sat) = \frac{W_N\mu_N C_{OX}\left(V_{OL}-V_{TN}-\frac{V_{OL}}{2}\right)V_{OL}}{L_N\left(1+\frac{V_{OL}}{E_{CN}L}\right)} = \frac{W_N(270)(1.6\times10^{-6})\left(1.2-0.4-\frac{0.1}{2}\right)0.1}{L_N\left(1+\frac{0.1}{0.6}\right)}$$ Pr

$$\frac{W_N}{L_N} = 38.5 \quad W_N = 77\lambda \qquad W_3 = 3\times77\lambda = 232\lambda \quad (3\,stack) \quad W_2 = 155\lambda \quad (2\,stack)$$

Problem 2 – P5.10



Problem 5.10 Continued

$$t_{PLH} = 0.7RC = R_{EQP}\frac{L}{W_P}C_{LOAD}$$

$$W_P = 0.7R_{EQP}\frac{L}{t_{PLH}}C_{LOAD} = 0.7\left(30\times10^3\right)\frac{(2\lambda)}{\left(50\times10^{-12}\right)}\left(75\times10^{-15}\right) = 63\lambda$$

$$t_{PHL} = RC = 0.7R_{EQN}\frac{L}{W_N}C_{LOAD}$$

$$W_N = 0.7R_{EQN}\frac{L}{t_{PHL}}C_{LOAD} = 0.7\left(12.5\times10^3\right)\frac{(2\lambda)}{\left(50\times10^{-12}\right)}\left(75\times10^{-15}\right) = 26.6\lambda \approx 27\lambda$$

Because the number of transistors in series is more than one, we must multiply the widths by the appropriate number. Here, all the NMOS transistors will have a width of 54λ. The PMOS transistors will have widths of 126λ and 190λ, respectively.

Problem 3 – P5.11

We estimate the dc power and dynamic switching power for this problem.

a.) The circuit's dc power can be computed by computing the dc current when the output is low. This is given by I_{DS}=550uA/um x 0.1um=55uA. Then P_{DC}=66uW when the output is low.

b.) Its dynamic power can be calculated by simply using the equation $P_{dyn} = \alpha C V_{DD}^2 f$. Therefore, P_{dyn}=(50fF)(V_{DD}-V_{TN})(V_{DD})(100MHz)=4.4uW.

Problem 4 – P5.12

The pseudo-NMOS inverter has static current when the output is low. We can estimate it as:

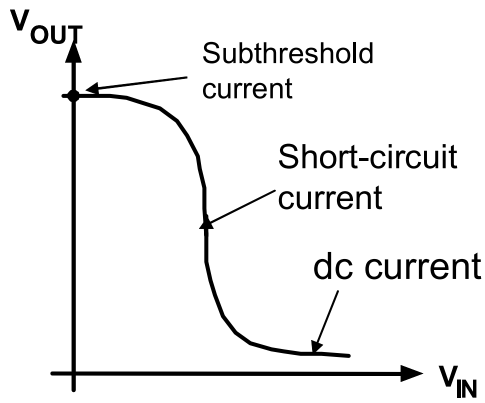
$$I_P(sat) = \frac{W_P v_{sat} C_{OX}\left(V_{GS}-V_T\right)^2}{V_{GS}-V_T+E_{CP}L} = \frac{\left(0.1\times10^{-4}\right)\left(8\times10^6\right)\left(1.6\times10^{-6}\right)\left(1.2-0.4\right)^2}{1.2-0.4+(24)(0.1)} = 25.6\mu\text{A}$$

Then the average static power is P_{stat} =(25.6uA)(1.2)/2 =15.4uW.

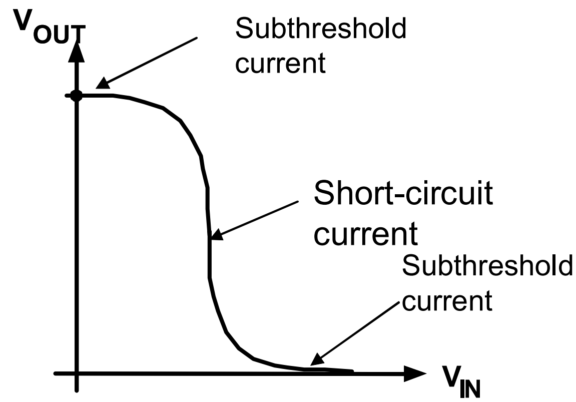
The dynamic power is $P_{dyn} = CV_{DD}V_{swing}f_{avg}$ =(50fF)(1.2)(1.1)f_{avg} assuming that V_{OL} is 0.1V.

For the CMOS inverter, the static power is almost zero: P_{stat}=$I_{sub}V_{DD}$. It is far less than the pseudo-NMOS case. The dynamic power $P_{dyn} = CV_{DD}V_{swing}f_{avg}$ =(50fF)$(1.2)^2f_{avg}$ is slightly larger than the pseudo-NMOS case.

Problem 5.12 - Continued



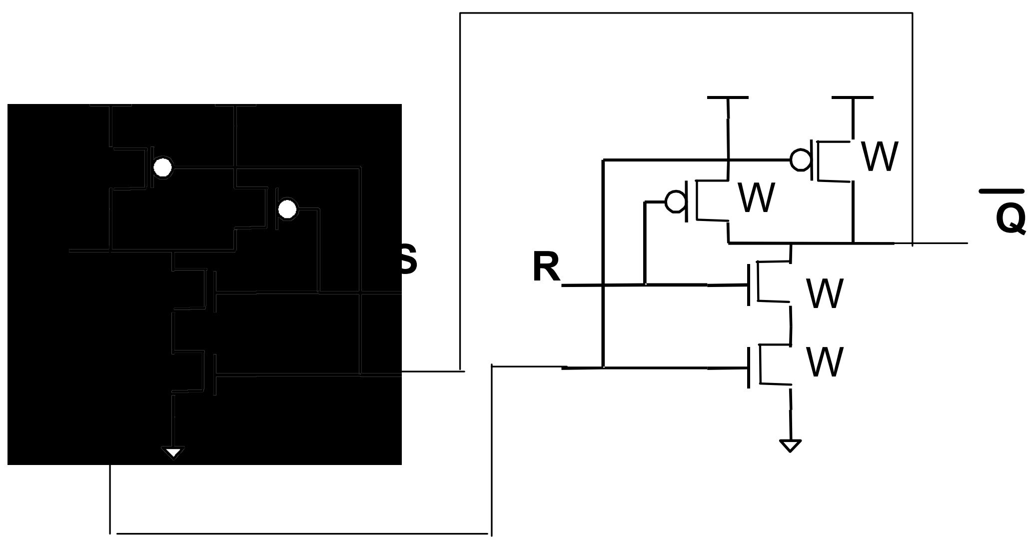
Pseudo-NMOS



CMOS Inverter

Problem 5 – P5.16

The circuit is shown below. The delay should incorporate both Q and Qb settling in 400ps. All NMOS and PMOS devices are the same size in both NAND gates.



$$t_P = t_{PHL} + t_{PLH} = 0.7R_{UP}C_{LOAD} + 0.7R_{DOWN}C_{LOAD} = 0.7C_{LOAD}\left(R_{eqp}\frac{L_P}{W_P} + R_{eqn}\frac{2L_N}{W_N}\right)$$

$$= \frac{0.7C_{LOAD}\left(R_{eqp}L + 2R_{eqn}L\right)}{W}$$

$$W = \frac{0.7C_{LOAD}\left(R_{eqp}L + 2R_{eqn}L\right)}{t_P} = \frac{0.7\left(100\times10^{-15}\right)\left(\left(30\times10^{3}\right)(0.1) + 2\left(12.5\times10^{3}\right)(0.1)\right)}{400\times10^{-12}}$$

$$\approx 1\mu\text{m}$$